Motion Control System

Hardware Manual

Revision 17.2

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1 DOCUMENT MANAGEMENT

1.1 Release

Issue	Date	Comments
2	13th November, 1992	Early release
3	7th December, 1992	6321 instead of 68230. Removed resolver i/f. Increased no of connectors. Interim release.
4	1st February, 1993	Major concept changes.
5	16th April, 1993	Detailed changes.
6	7th July, 1993	Schematics developed.
7	17th July, 1993	Detailed changes.
8	9th August, 1993	Second board revision
9	14th December, 1993	Third host revision
10	3rd February, 1995	Stepper on slave Rev B
11	27th February, 1995	Detailed changes.
12	2nd May, 1995	Revision E Host Control Board
13	16th April, 1996	Revision F Host Control Board
14	1st November, 1996	3 slot backplane
15	July, 1998	Operator interface
16	April, 2001	Rev F PC3/120 control board
17	June, 2001	Rev D PC3/110 control board

2 INTRODUCTION

This document describes the hardware specification for a family of circuit boards, designed for real time control, and in particular motion control applications. The functionality, and software is described in the appropriate user manual.

3 SYSTEM OVERVIEW

The system is designed to offer a solution for a wide range of industrial control and monitoring applications. The system is based on circuit boards which can be enclosed in a range of different enclosures. The system is able to control the positions of up to eight motors (closely coupled). The motors & drives can be any form of linear analogue system (e.g. DC servo, inverter drive) with position feedback. In addition any of the motors can be a stepper motor. Position feedback is in the form of an incremental optical encoder as standard. Serial absolute encoders can be connected to the daughter board, and there will be an option for resolver feedback.

The system is broadly divided into the motion controller and the operator interface. These are loosely coupled by means of an asynchronous serial link. All inputs and outputs (with a few exceptions) are optically isolated.

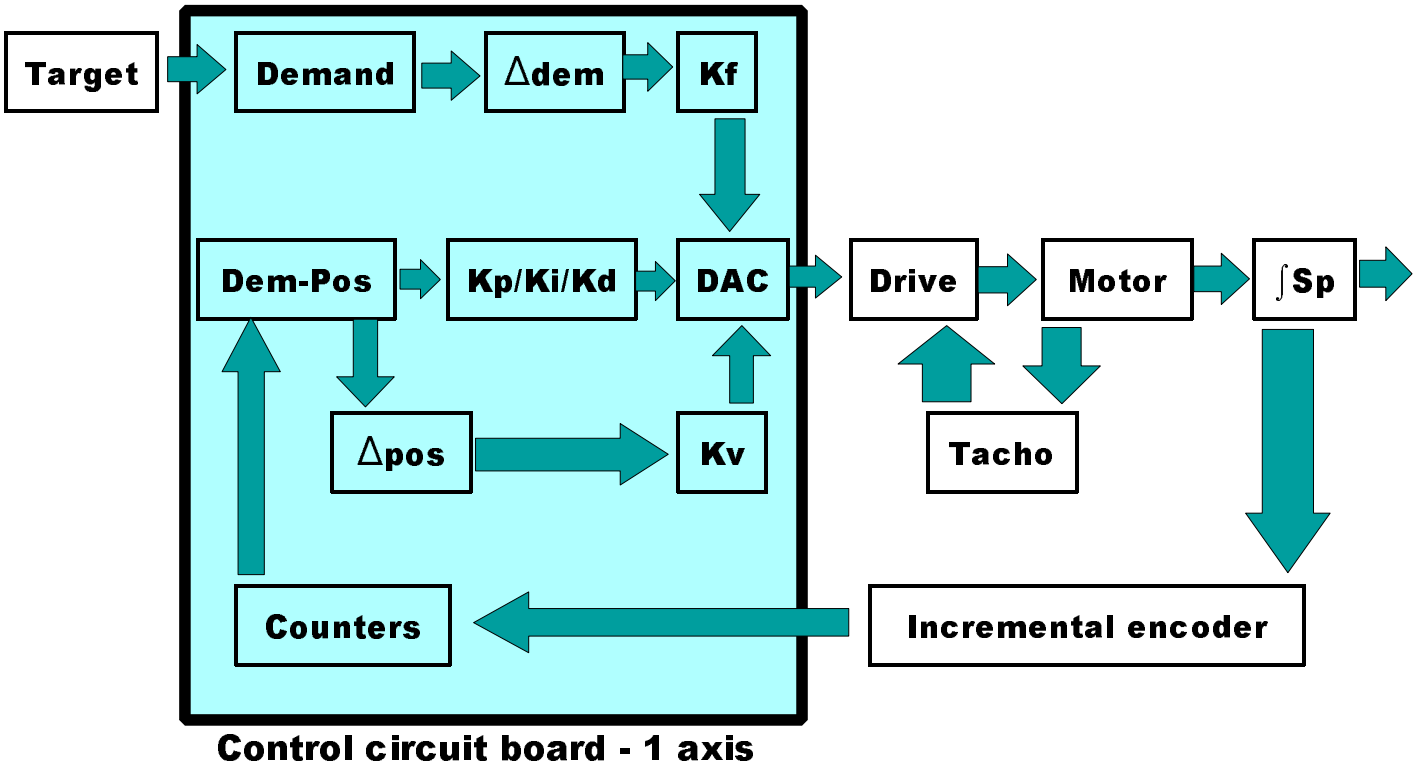
The motion controller consists of a microcontroller based host control board (2 axes) connected to one or more slave control boards (2 axes each) by means of a G-64 computer bus. Each control board has 8 parallel inputs and 8 outputs as standard. Also, each control board can accommodate up to two daughter boards for additional inputs and outputs, position feedback options, displays, etc.). Each axis has 2 analogue outputs and one incremental encoder interface. The host control board also has the facility to control 2 stepper motors (sacrificing 4 of the standard parallel output lines), and two isolated and 6 non-isolated 10-bit analogue inputs. The system can be set up using the serial port of a personal computer.

The operator interface consists of a microcontroller based circuit board, which can accommodate one daughter board (of the same type which the motion controller can accommodate). The operator interface board has 8 parallel inputs and 8 outputs, together with an incremental encoder interface. It also has a number of analogue inputs and counter/timer inputs & outputs (not isolated). In addition, it has a G-64 bus for communication with other G-64 bus based circuit boards.

Currently there is only one daughter board, which provides upto four isolated RS-422/485 serial links, together with driver for upto four numerical L.E.D. (7 segment) displays (each of up to 8 digits). There are two alternative display boards currently available, both based on 14.2mm high 7 segment L.E.D. displays. One has 8 digits (plus decimal point), and the other has 5 digits (plus decimal point).

There are plans to produce a number of new daughter boards, to provide the following functionality.

1. Resolver feedback.
2. Fibre optic serial links.
3. More parallel i/o (e.g. for thumbwheel switches).



The control system works on the basis of continually sampling information and performing a control algorithm at a defined timer interval (known as the sampling time). This sampling time is set to be 1÷256th second. In other words, the time interval between updating calculations is about 3.9ms. The control software uses two key pieces of information to generate a positional error. These are the current demanded position, and the current measured position. The demanded position is calculated by the controller on the basis of a target positional move. For example, if the controller is asked to move a distance of 4000 encoder counts at a speed of 500 counts/sec and an acceleration of 2000 counts/sec², it can generate a velocity profile in terms of the desired position at every 1÷256th second. If the system is under control but not moving, there is still be a demand position, but it does not change.

This positional error information is used as the basis for a *PID* (proportional, integral, and derivative) calculation, whose output is fed to a Digital to Analogue Converter (DAC). The analogue voltage is sent to an analogue drive as a velocity command.

Most high performance drive systems have an analogue velocity control loop built in. This takes the form of a Tacho-generator on the end of the motor shaft, which generates a voltage proportional to its velocity, and an associated gain potentiometer on the drive. This allows a stable, high gain system to be set-up.

The system is intended for use with digital incremental position encoders which provide two signals in quadrature. The encoder interface multiplies the resolution of the encoder by four, such that each complete cycle of the encoder signals represents four counts.

The encoder signals are decoded and counted by hardware on the control board. The software converts these to numbers which represent the measured position. This signal is then used to compare with the demanded position information, as described above.

The system is set up by high level commands from a serial link. Most commands are two letters, sometimes followed by a numerical parameter. These commands can be built up into programmes which can then be stored on non-volatile memory (Flash memory) on the system. The motors may be controlled using simple proportional control, where the demand signal depends on only the position error. The proportional gain constant is set by the user. It is also possible for the user to set gain constants for integral feedback, differential feedback, velocity feedback, and velocity feed-forward terms, providing very flexible control over the system transfer function.

All boards are powered from a 5v & ±15v switched mode power supply of sufficient capacity. No cooling fan is necessary, and CMOS devices are used wherever possible.

The control software is highly deterministic, being interrupt driven by a hardware timer. The control algorithm is implemented every time this hardware timer generates an interrupt (every 1÷256 second). In addition, polling of the external inputs is carried out during the same servo loop closure process. Serial character receipt and transmission is also handled by the interrupt mechanism, and a special high priority interrupt is used for reference marker detection. This gives a response time of better than 15µs.

The command interpreter is executed in background mode, together with display routines.

The modular approach to the software means that system can be easily adapted to particular situations.

3.2 Circuit boards

3.2.1 Host control board (PC3/100, Revision F).

This provides feedback position control for up to 2 axes. It is based on the Motorola MC68HC16Z1 microprocessor. Its functions include:

(i) Up to 4 channels D to A output (12 bits resolution). All channels are isolated against high voltage. Bipolar -10/+10v output.
(ii) 8 channels A to D input (10 bits resolution). These channels are not isolated, and must be in the range 0-5v.
(iii) 2 channels Quadrature & ref input. Isolated RS-422 inputs (differential signals).
(iv) 16 channels of general purpose parallel inputs (4 of which may be used for reference inputs). Isolated inputs. Default to 24v DC, with selectable alternative voltages. 8 of these inputs can be re-defined as outputs.
(v) 16 channels of general purpose parallel outputs. Isolated output. Output voltage supplied externally. 8 of these outputs can be re-defined as inputs.
(vi) 4 asynchronous serial ports. TTL signals to daughter board. One of these is also taken to an isolated RS-485/422 circuit for use on a proprietry bus, or general purpose RS-422.
(vii) Real time clock.
(viii) Hardware watchdog.
(ix) 1 dedicated Asynchronous RS-232 serial port (set-up terminal)
(x) Memory sockets to allow a mix of SRAM and Flash memory. Also serial EEPROM and NOVRAM.
(xi) Programmable logic to be used for i/o line logic and address & chip select decoding.
(xii) Synchronous & asynchronous extended G-64 bus interface (with option for 1 or 2 MHz operation). Allows synchronous serial/8-bit data bus/chip select connections to slave control board
(xiii) Isolated CAN bus.
(xiv) IBM AT keyboard interface.
(xv) Scanning keypad interface.
(xvi) LCD display interface.
(xvii) Two channels SSI serial absolute position feedback interface.
(xviii) Two channels remote resolver absolute position feedback interface.
(xix) Sites for 2 single Euromodule sized daughter boards.
(xx) Site for one front edge daughter board.

3.2.2 Slave control board (PC3/110, Revision D).

This provides feedback position control for up to 2 axes. It is a slave to the central control board (and uses the central control board's microprocessor). Its functions include:

(i) 4 channels D to A output (12 bits resolution). All channels are be isolated against high voltage. Bipolar (-10/+10v or unipolar (0/+10v) selectable.
(ii) 3 channels Quadrature & ref input. Isolated inputs, with differential signals from 0 to 24 volts.
(iii) 8 channels of general purpose parallel inputs (8 of which may be used for reference inputs). Isolated inputs. Default to 24v DC, with selectable alternative voltages.
(iv) 8 channels of general purpose parallel outputs. Isolated output. Output voltage supplied externally.
(v) 4 asynchronous serial ports. TTL signals to daughter board.
(vi) Synchronous serial/8-bit data bus/chip select connections to host control board

3.2.3 Operator interface and value controller board (PC3/120, revision F).

This is a microprocessor driven circuit board, based on a Motorola 68HC11 microprocessor. It communicates with the host control board by an asynchronous serial port. It will allow for a matrix keyboard to be connected.

3.2.4 Serial driver/display board (PC3/130). This is a daughter board to the host/slave control board, or the operator interface board. It provides up to 4 isolated RS-422 duplex channels and up to 4 seven segment L.E.D. driver units (each with up to 8 digits).

3.2.5 Auxiliary control board (PC3/135). This is a daughter board to the host/slave control board. Its functions include:

(i) 4 channels D to A output (12 bits resolution). All channels are isolated against high voltage. Bipolar (-10/+10v or unipolar (0/+10v) selectable.
(ii) 2 channels Quadrature & ref input. Isolated RS-422 inputs (differential signals).
(iii) 16 channels of general purpose parallel inputs (4 of which may be used for reference inputs). Isolated inputs. Default to 24v DC, with selectable alternative voltages. 8 of these inputs can be re-defined as outputs.
(iv) 16 channels of general purpose parallel outputs. Isolated output. Output voltage supplied externally. 8 of these outputs can be re-defined as inputs.
(v) Hardware watchdog.
(vi) Programmable logic to be used for i/o line logic and address & chip select decoding.
(vii) Two channels SSI serial absolute position feedback interface.
(viii) Two channels remote resolver absolute position feedback interface.

3.2.6 L.E.D. display board (PC3/140). This consists of 5 seven segment L.E.D. displays (14.2mm). It is connected to the serial driver/display board by means of a ribbon cable.

3.2.7 L.E.D. display board (PC3/141). This consists of 8 seven segment L.E.D. displays (14.2mm). It is connected to the serial driver/display board by means of a ribbon cable.

3.2.8 Counter/timer board (TIO-33). This is used for controlling open loop stepper drives. It is connected by means of a DIN 41612 connector at the rear of the board.

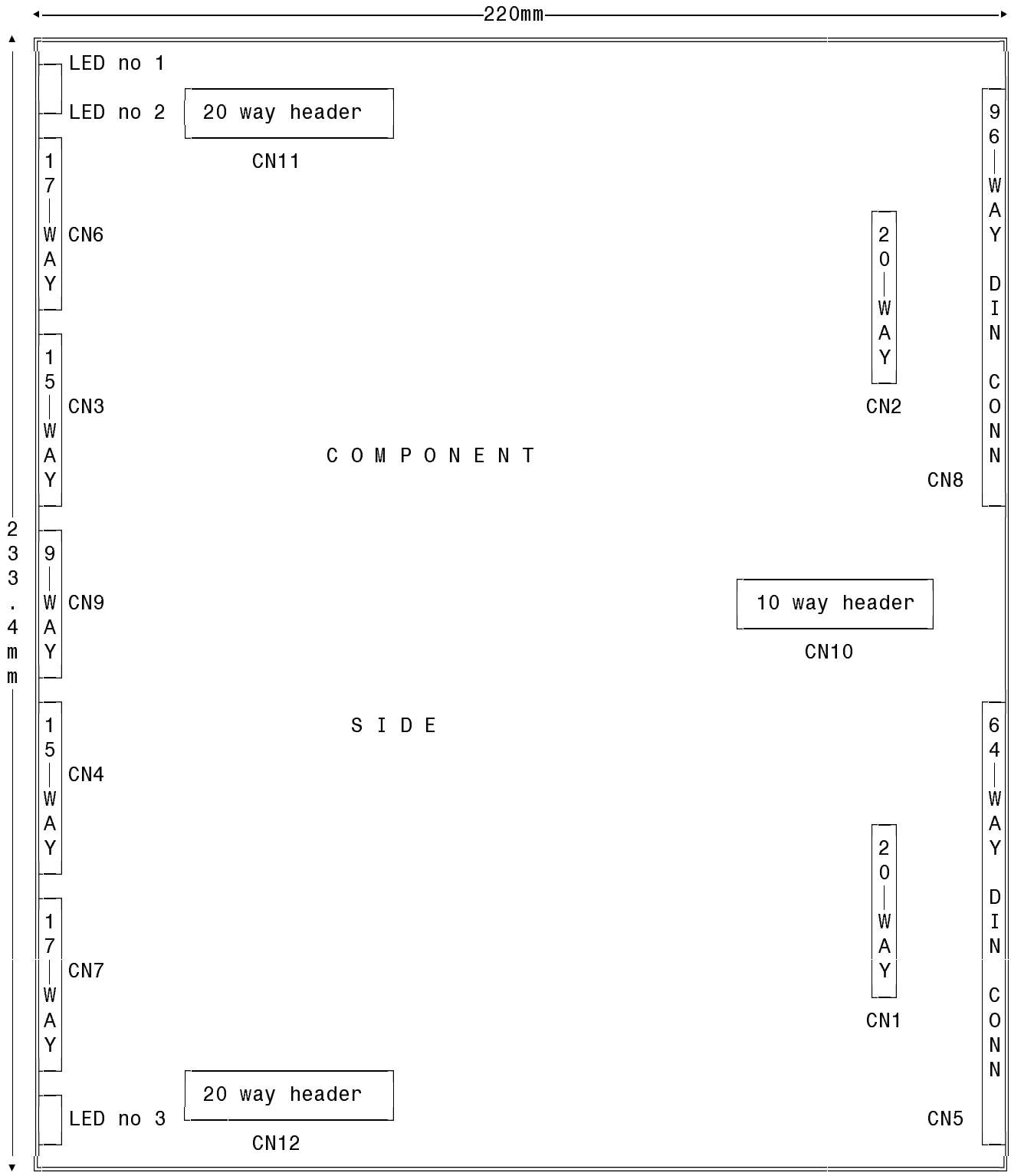
3.2.9 G-64 bus, 3 slot (PC3/152). This is used for a connecting host control (PC3/100) to a slave control (PC3/110) board.

3.2.10 G-64 bus, 4 slot (PC3/153) & power supply This is used for a connecting host control (PC3/100) to up to 3 slave control (PC3/110) boards. It also provides power form an ac main supply, and has various i/o connectors.

3.2.11 Analogue input (PC3/155). This provides isolated signal conditioning (0-10V or 0-±10V) on up to 8 channels.

3.3 Host Control (PC3/100) Rev F connectors & jumpers

There are twelve connectors on the board as follows:



The height of the board is double Eurocard size (233.4mm).

The general arrangement is as follows:

(i) Connector 1 - 20 way header for daughter board no 1.
(ii) Connector 2 - 20 way header for daughter board no 2.
(iii) Connector 3 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 1).
(iv) Connector 4 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 2).
(v) Connector 5 - 64 way DIN 41612 type B (rows a & b). G-64 synchronous computer bus & asynchronous serial.
(vi) Connector 6 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated inputs.
(vii) Connector 7 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated outputs.
(viii) Connector 8 - 96-way DIN 41612 type C (rows a & c). Isolated analogue inputs & timer inputs & outputs.
(ix) Connector 9 - 9-way D connector, for RS-232 serial connections.
(x) Connector 10 - 10 way header, for background mode debugging.
(xi) Connector 11 - 20 way header for front daughter board.
(xii) Connector 12 - 20 way header for front daughter board.

3.3.2 Connector 1. 20-way header for daughter board.

1 0 volts
2 XR-82C684 TXDA (Tx Asynchronous port 1)
3 XR-82C684 RXDA (Rx Asynchronous port 1)
4 XR-82C684 TXDB (Tx Asynchronous port 2)
5 XR-82C684 RXDB (Rx Asynchronous port 2)
6 5 volts
7 XR-82C684 TXDC (Tx Asynchronous port 3)
8 XR-82C684 RXDC (Rx Asynchronous port 3)
9 MC68HC16 TXD (Tx Asynchronous port 4)
10 MC68HC16 RXD (Rx Asynchronous port 4)
11 IRQD2
12 MC68HC16 MOSI (Tx Synchronous port)
13 MC68HC16 MISO (Rx Synchronous port)
14 MC68HC16 SCK (CLK Synchronous port)
15 MC68HC16 /RESET
16 MC68HC16 PCS1 (Synchronous port chip select)
17 MC68HC16 PCS0 (Synchronous port chip select)
18 MC68HC16 PCS2 (Synchronous port chip select)
19 MC68HC16 PCS3 (Synchronous port chip select)
20 MC68HC16 ECLOCK

3.3.3 Connector 2. 20-way header for daughter board.

1 0 volts
2 XR-82C684 TXDA (Tx Asynchronous port 1)
3 XR-82C684 RXDA (Rx Asynchronous port 1)
4 XR-82C684 TXDB (Tx Asynchronous port 2)
5 XR-82C684 RXDB (Rx Asynchronous port 2)
6 5 volts
7 XR-82C684 TXDC (Tx Asynchronous port 3)
8 XR-82C684 RXDC (Rx Asynchronous port 3)
9 MC68HC16 TXD (Tx Asynchronous port 4)
10 MC68HC16 RXD (Rx Asynchronous port 4)
11 IRQD2
12 MC68HC16 MOSI (Tx Synchronous port)
13 MC68HC16 MISO (Rx Synchronous port)
14 MC68HC16 SCK (CLK Synchronous port)
15 MC68HC16 /RESET
16 MC68HC16 PCS1 (Synchronous port chip select)
17 MC68HC16 PCS0 (Synchronous port chip select)
18 MC68HC16 PCS2 (Synchronous port chip select)
19 MC68HC16 PCS3 (Synchronous port chip select)
20 MC68HC16 ECLOCK

3.3.4 Connector 3. Position encoder, reference i/p, analogue o/p.

1 Ch.1 encoder track A
2 Ch.1 encoder track A
3 Ch.1 encoder track B
4 Ch.1 encoder track B
5 Ch.1 encoder track Z
6 Ch.1 velocity isolated supply (+15v) VR1
7 Ch.1 velocity isolated supply (-15v) VT1
8 Ch.1 encoder power supply 0v EVS1
9 Ch.1 encoder power supply +ve EVR1
10 Ch.1 encoder track $\bar{Z}$
11 Ch.1 velocity signal (DAC port A) AVEL
12 Ch.1 DAC aux. output (DAC port C) CAUX
13 Ch.1 velocity isolated supply 0v VS1
14 Ch.1 Relay Common 1COM
15 Ch.1 Relay normally open or normally closed (jumper selectable) 1CON

3.3.5 Connector 4. Position encoder, reference i/p, analogue o/p.

1 Ch.2 encoder track A
2 Ch.2 encoder track A
3 Ch.2 encoder track B
4 Ch.2 encoder track B
5 Ch.2 encoder track Z
6 Ch.2 velocity isolated supply (+15v) VR2
7 Ch.2 velocity isolated supply (-15v) VT2
8 Ch.2 encoder power supply 0v EVS2
9 Ch.2 encoder power supply +ve EVR2
10 Ch.2 encoder track $\bar{Z}$
11 Ch.2 velocity signal (DAC port B) BVEL
12 Ch.2 DAC aux. output (DAC port D) DAUX
13 Ch.2 velocity isolated supply 0v VS2
14 Ch.2 Relay Common 2COM
15 Ch.2 Relay normally open or normally closed (jumper selectable) 2CON

3.3.6 Connector 5.

G-64 bus signals and functions

Details of the G-64 bus signals and their functions are shown below. A '/' prefix on the signal name denotes an active low signal. A '*' in the "Used" column indicates the signals which are used on this board. A '**' indicates that the signals are used and that they differ from the G-64 standard.

Pin	Signal	I/O	Used	Function
1a	GND	O	✶	0V supply
1b	GND	O	✶	0V supply
2a	A0	O	✶	Address bit 0 (least significant) Address outputs from processor board.
2b	A8	O	✶	Address bit 8
3a	A1	O	✶	Address bit 1
3b	A9	O	✶	Address bit 9
4a	A2	O	✶	Address bit 2
4b	$\overline{PCS0}$	O	✶✶	SPI chip select 0 The SPI chip selects can be decoded to provide 15 individual chip selects.
5a	A3	O	✶	Address bit 3
5b	$\overline{PCS1}$	O	✶✶	SPI chip select 1
6a	A4	O	✶	Address bit 4
6b	$\overline{PCS2}$	O	✶✶	SPI chip select 2
7a	A5	O	✶	Address bit 5
7b	$\overline{PCS3}$	O	✶✶	SPI chip select 3
8a	A6	O	✶	Address bit 6
8b	SCK	O	✶✶	SPI synchronous clock
9a	A7	O	✶	Address bit 7
9b	MOSI	O	✶✶	SPI Master Out Slave In
10a	BGRT	O		Bus Grant
10b	$\overline{BRQ}$	I		Bus Request
11a	$\overline{REFGNT}$	I/O		Refresh cycle grant
11b	$\overline{REFREQ}$	I/O		Refresh cycle request
12a	$\overline{HALT}$	I/O		Halt processor
12b	$\overline{BGACK}$	I/O		Bus Grant Acknowledge
13a		SYS	O	System clock
13b	ECLOCK	O	✶	E clock Data transfer takes place when E is high
14a	$\overline{VPA}$	O	✶	Valid Peripheral Address
14b	$\overline{RES}$	O	✶	System Reset signal

Pin	Signal	I/O	Used	Function
15a	$\overline{DTACK}$	I/O	✶	Data Transfer Acknowledge signal.
15b	$\overline{NMI}$	I	✶	Non-Maskable Interrupt
16a	$\overline{AS}$	O	✶	Address Strobe
16b	$\overline{IRQ}$	O	✶	Interrupt Request
17a	R/$\overline{W}$	O	✶	Read/Write.
17b	$\overline{FIRQ}$	I/O	✶	Fast Interrupt Request
18a	HALTACK	O		Halt Acknowledge
18b	IACK	O	✶	Interrupt Acknowledge
19a	$\overline{D8}$	I/O	✶	Data bit 8.
19b	$\overline{D12}$	I/O	✶	Data bit 12.
20a	$\overline{D9}$	I/O	✶	Data bit 9.
20b	$\overline{D13}$	I/O	✶	Data bit 13.
21a	$\overline{D10}$	I/O	✶	Data bit 10.
21b	$\overline{D14}$	I/O	✶	Data bit 14.
22a	$\overline{D11}$	I/O	✶	Data bit 11.
22b	$\overline{D15}$	I/O	✶	Data bit 15 (most significant).
23a	$\overline{D0}$	I/O	✶	Data bit 0 (least significant).
23b	$\overline{D4}$	I/O	✶	Data bit 4.
24a	$\overline{D1}$	I/O	✶	Data bit 1.
24b	$\overline{D5}$	I/O	✶	Data bit 5.
25a	$\overline{D2}$	I/O	✶	Data bit 2.
25b	$\overline{D6}$	I/O	✶	Data bit 6.
26a	$\overline{D3}$	I/O	✶	Data bit 3.
26b	$\overline{D7}$	I/O	✶	Data bit 7.
27a	MISO	I	✶✶	SPI Master In Slave Out
27b	PERR	I		Parity Error/ Bus Error
28a	CH.OUT	O		Daisy chain output
28b	CH.IN	I		Daisy chain input
29a	-5V	I		-5V supply
29b	+5V BAT	I		+5v supply from standby battery
30a	+15V	I	✶✶	+15V supply
30b	-15V	I	✶✶	-15V supply
31a	+5V	I	✶	+5V supply
31b	+5V	I	✶	+5V supply
32a	GND	I	✶	0V supply
32b	GND	I	✶	0V supply

3.3.7 Connector 6. 17 way PCB header, Klippon type SL3.5/17/90. Isolated inputs.

1	Input common (0v)
2	Input 1
3	Input 2
4	Input 3
5	Input 4
6	Input 5
7	Input 6
8	Input 7
9	Input 8
10	Input 9
11	Input 10
12	Input 11
13	Input 12
14	Input 13
15	Input 14
16	Input 15
17	Input 16

3.3.8 Connector 7. 17 way PCB header, Klippon type SL3.5/17/90. Isolated outputs (or outputs **and** inputs if LK26 is connected, and optocouplers are correctly set up).

1	Output common (24v DC)
2	Output 1
3	Output 2
4	Output 3
5	Output 4
6	Output 5
7	Output 6
8	Output 7
9	Output 8
10	Output 9 or Input 17
11	Output 10 or Input 18
12	Output 11 or Input 19
13	Output 12 or Input 20
14	Output 13 or Input 21
15	Output 14 or Input 22
16	Output 15 or Input 23
17	Output 16 or Input 24

3.3.9 Connector 8. Analogue inputs & timer inputs and outputs. 96-way DIN 41612 type C (rows a & c).

1a	Stepper channel 1 clock
1c	Stepper channel 1 direction
2a	Stepper channel 2 clock
2c	Stepper channel 2 direction
3a	Stepper channel 3 clock
3c	Stepper channel 3 direction
4a	Stepper channel 4 clock
4c	Stepper channel 4 direction
5a	Keypad processor B0
5c	Keypad processor A0
6a	Keypad processor B1
6c	Keypad processor A1
7a	Keypad processor B2
7c	Keypad processor A2
8a	Keypad processor B3
8c	Keypad processor A3
9a	Keypad processor B6
9c	Keypad processor NMI
10a	Keypad processor B7
10c	CAN interface RX1
11a	CAN interface TX0
11c	CAN interface RX0
12a	Chip select LCD display
12c	LCD display clock
13a	LCD display data 0
13c	LCD display data 1
14a	LCD display data 2
14c	LCD display data 3
15a	LCD display data 4
15c	LCD display data 5
16a	LCD display data 6
16c	LCD display data 7
17a	XR-82C684 OP10
17c	XR-82C684 IP8
18a	XR-82C684 TXDC
18c	XR-82C684 RXDC
19a	XR-82C684 TXDB
19c	XR-82C684 RXDB
20a	XR-82C684 TXDA
20c	XR-82C684 RXDA
21a	MC68HC16 TXD
21c	MC68HC16 RXD
22a	MC68HC16 OC1
22c	MC68HC16 IC1
23a	MC68HC16 OC2
23c	MC68HC16 IC3
24a	MC68HC16 OC4
24c	MC68HC16 IC4
25a	MC68HC16 PAI
25c	MC68HC16 PCLK
26a	MC68HC16 PWMB
26c	MC68HC16 PWMA
27a	0v digital (non-isolated)
27c	0v digital (non-isolated)
28a	0v analogue (non-isolated)
28c	0v analogue (non-isolated)
29a	MC68HC16 Analogue input 0
29c	MC68HC16 Analogue input 1

30a MC68HC16 Analogue input 2
30c MC68HC16 Analogue input 3
31a MC68HC16 Analogue input 4
31c MC68HC16 Analogue input 5
32a MC68HC16 Analogue input 6
32c MC68HC16 Analogue input 7

3.3.10 Connector 9. 9-way RS-232 D-type connector (female)

1 Not used
2 RS-232 serial port TX (XR-82C684 ch D) - Output
3 RS-232 serial port RX (XR-82C684 ch D) - Input
4 Not used
5 RS-232 serial port GND
6 Not used
7 RS-232 serial port CTS (XR-82C684 ch D i/p 9) - Input
8 RS-232 serial port RTS (XR-82C684 ch D o/p 9) - Output
9 Not used

Connections for cable for IBM compatible Personal Computer:

	9-pin plug(Controller)		25-pin socket(PC)	9-pin socket (PC)	
	2	->	3	2	RX
	3	<-	2	3	TX
	5	<->	7	5	GND
Hardware)	7	<-	4	7	RTS
Handshake)	8	->	5	8	CTS
Connect these 4	)	->	8	1	DCD
lines together	)	->	6	6	DSR
when using hardware)	->	22	9	RI	
handshaking)	<-	20	4	DTR	

Connections for cable for US Robotics 56K FaxModem:

	9-pin plug(Controller)		25-pin plug(PC)		
	2	->	2	RX	
	3	<-	3	TX	
	5	<->	1	GND	
Hardware)	7	<-	5	RTS	
Handshake)	8	->)	4	CTS	) Link to 20
		)	20		) Link to 4

3.3.11 Connector 10. 10-way header for background mode debugging.

1 DS
2 BERR
3 GND
4 DSCLK
5 GND
6 FREEZE
7 RESET
8 DSI
9 VDD
10 DSO

3.3.12 Connector 11. 20-way header for front daughter board.

1 0 volts (Digital)
2 MC68HC16 Address bit 0
3 MC68HC16 Address bit 1
4 MC68HC16 Address bit 2
5 MC68HC16 Address bit 3
6 5 volts
7 MC68HC16 R/W
8 Chip select VIA's
9 Chip select Quadrature decoder 1
10 MC68HC16 /RESET
11 CLOCKDEC
12 MC68HC16 Data bit 8
13 MC68HC16 Data bit 9
14 MC68HC16 Data bit 10
15 MC68HC16 Data bit 11
16 MC68HC16 Data bit 12
17 MC68HC16 Data bit 13
18 MC68HC16 Data bit 14
19 MC68HC16 Data bit 15
20 MC68HC16 ECLOCK

3.3.13 Connector 12. 20-way header for front daughter board.

1 0 volts (digital)
2 65C22 CA1
3 +15 volts
4 -15 volts
5 0 volts (analogue)
6 5 volts
7 65C22 CB1
8 65C22 CB2
9 MC68HC16 Address bit 4
10 Chip select PTM's
11 IRQDF
12 MC68HC16 MOSI (Tx Synchronous port)
13 MC68HC16 MISO (Rx Synchronous port)
14 MC68HC16 SCK (CLK Synchronous port)
15 Chip select Quadrature decoder 2
16 MC68HC16 PCS1 (Synchronous port chip select)
17 MC68HC16 PCS0 (Synchronous port chip select)
18 MC68HC16 PCS2 (Synchronous port chip select)
19 MC68HC16 PCS3 (Synchronous port chip select)

20 65C22 CA2

3.3.14 Jumper definitions.

Jumper	Function	Connections
1	Relay N/O (ch1) to pin 15 of conn 3	1-2
	Relay N/C (ch1) to pin 15 of conn 3	2-3
2	E clock (A23 of 68HC16, U59) to display clock (pin 8, U54)	1-2
	1/E clock (pin27, U64) to display clock (pin 8, U54)	2-3
3	PC3100G (U10) pin 19 to NMI (U17)	1-2
	3Y (U13) to NMI (U17)	2-3
4	0v to Relay enable (DAC)	1-2
	Watchdog OK Relay enable (DAC)	2-3
5	By-pass analogue output isolation for channel 1	1-2
	Use ISO122 analogue isolation amplifier for channel 1	2-3
6	MAX232 (U31) pin 12 to 68HC16 (U59) pin 17 & Jumper 8 pin 3	1-2
	MAX232 (U31) pin 12 to 82C684 (U57) pin 27 & Jumper 8 pin 1	2-3
7	CN1/2 pin 10 to 82C684 (U57) pin 27 & Jumper 6 pin 3	1-2
	CN1/2 pin 10 to 68HC16 (U59) pin 17 & Jumper 6 pin 1	2-3
8	MAX232 (U31) pin 11 to 68HC16 (U59) pin 18 & Jumper 12 pin 3	1-2
	MAX232 (U31) pin 11 to 82C684 (U57) pin 28 & Jumper 12 pin 1	2-3
9	By-pass analogue output isolation for channel 1 auxiliary	1-2
	Use ISO122 analogue isolation amplifier for channel 1 aux	2-3
10	0v to Relay enable (PTM's)	1-2
	Watchdog OK Relay enable (PTM's)	2-3
11	By-pass analogue output isolation for channel 2	1-2
	Use ISO122 analogue isolation amplifier for channel 2	2-3
12	CN1/2 pin 9 to jumper 8 pin 3	1-2
	CN1/2 pin 9 to 68HC16 (U59) pin 18 & Jumper 8 pin 1	2-3
13	Relay N/O (ch2) to pin 15 of conn 4	1-2
	Relay N/C (ch2) to pin 15 of conn 4	2-3
14	By-pass analogue output isolation for channel 2 auxiliary	1-2
	Use ISO122 analogue isolation amplifier for channel 2 aux	2-3
15	MISO (68HC16) to U42 pin 12	1-2
	MISO (68HC16) to U35 pin 12	2-3
16	Plant i/p line 2 to Ref input 2	1-2
	Encoder ref signal to Ref input 2	2-3
17	82C684 (U57) pin 32 to jumper 19 pin 1	1-2
	82C684 (U57) pin 32 to PC3100F (U63) pin 1	2-3
18	Plant i/p line 1 to Ref input 1	1-2
	Encoder ref signal to Ref input 1	2-3
19	Pins 10, 12, 14, 16 of U73 & 75 to U55 & 62 (16 i/p & 16 o/p)	1-2
	Pins 10, 12, 14, 16 of U73 & 75 to CN6 pin 1 (24 i/p & 8 o/p)	2-3
20	PC3100A (U58) pin 20 to OC2 (68HC16)	1-2
	PC3100A (U58) pin 20 to 0v	2-3
21	PC3100A (U58) pin 42 to IC4 (68HC16)	1-2
	PC3100A (U58) pin 42 to 0v	2-3
22	VSTBY (68HC16) to battery supply	1-2
	VSTBY (68HC16) to 0v	2-3
23	ADA7 (68HC16) to conn 8 pin 8C	1-2
	ADA7 (68HC16) to battery	2-3
24	U48 pin 9 to PC3100B (U64) pin 2	1-2
	U48 pin 9 to PC3100D (U9) pin 13	2-3
25	512K SRAM	1-2
	128K SRAM	2-3
26	LCD display power supply trimmer to -VA	1-2
	LCD display power supply trimmer to VCC	2-3
27	512K SRAM	1-2
	128K SRAM	2-3
28	0v to PTM gate 23	1-2
	Relay enable (PTM's) to PTM gate 23	2-3

29	0v to PTM gate 22	1-2
	Relay enable (PTM's) to PTM gate 22	2-3
30	0v to PTM gate 21	1-2
	Relay enable (PTM's) to PTM gate 21	2-3
31	0v to PTM gate 13	1-2
	Relay enable (PTM's) to PTM gate 13	2-3
32	0v to PTM gate 12	1-2
	Relay enable (PTM's) to PTM gate 12	2-3
33	0v to PTM gate 11	1-2
	Relay enable (PTM's) to PTM gate 11	2-3
34	Chip Select (LCD) to Output enable of U76	1-2
	Chip Select (LCD) to 0v	2-3

3.3.15 Link definitions.

Link	Function		Connections
1	Pin 3 (1Y) of U13	/	1
	Pin 1 (1A) of U13	\	2
2	0V isolated to ASC of U15		1-2
3	0V to PC3100D (U9) pin 9		1-2
4	ISO RD LED (U22) to PC3100D (U9) pin 11		1-2
5	+5V to conn 3 pin 9		1-2
6	0VA to conn 3 pin 13		1-2
7	+5V to pin 8 of U44 (RS-485)		1-2
8	0V to TIM of U37		1-2
9	C23 of PTM (U77) to B6 of U45		1-2
10	PAI of 68HC16 (U59) to B7 of U45		1-2
11	PCLK of 68HC16 (U59) to B5 of U45		1-2
12	0V to FS of U22		1-2
13	0V to DSACK1 (PE5) of 68HC16 & pin 5 of U22		1-2
14	0V to DE & /RE (U44)		1-2
15	ISO RD DRV (U22) to R (U44)		1-2
16	0V to conn 3 pin 8		1-2
17	+5V (isolated) to conn 8 pin 16c		1-2
18	0VA to conn 4 pin 13		1-2
19	+5V to conn 4 pin 9		1-2
20	VREFA of U35 to VREFA of U42		1-2
21	Ref input 2 to IP11 (QUART)		1-2
22	Ref input 2 to CB1 (VIA)		1-2
23	Ref input 2 to IC2 (68HC16)		1-2
24	C13 of PTM (U80) to B4 of U45		1-2
25	0V to conn 4 pin 8		1-2
26	0V to IP15 (QUART)		1-2
27	0V to IP14 (QUART)		1-2
28	0V to IP13 (QUART)		1-2
29	0V to IP12 (QUART)		1-2
30	Ref input 1 to IP10 (QUART)		1-2
31	Ref input 1 to CA1 (VIA)		1-2
32	Ref input 1 to IC1 (68HC16)		1-2
33	0v to pin 23 of PC3100G (U10)		1-2
34	Q2 of U48 \	/	1
	Q5 of U48 /	\	2
35	68HC16 clock from RTC		1-2
36	IC3 (68HC16) TO OC3 (68HC16)		1-2
37	C11 of PTM (U80) to no connection		1-2
38	C22 of PTM (U77) to no connection		1-2
39	C12 of PTM (U80) to no connection		1-2
40	C21 of PTM (U77) to no connection		1-2

41	VBT to conn 5 pin 28B	1-2

3.3.16 Default jumper settings.

This shows the default (factory) settings for the jumpers for a PC3/100 host control board:

JUMPER 1 1·-· ·3
JUMPER 2 1· · ·3
JUMPER 3 1· ·-·3
JUMPER 4 1· ·-·3
JUMPER 5 1· ·-·3
JUMPER 6 1· ·-·3
JUMPER 7 1· · ·3
JUMPER 8 1· ·-·3
JUMPER 9 1· ·-·3
JUMPER 10 1·-· ·3
JUMPER 11 1· ·-·3
JUMPER 12 1· · ·3
JUMPER 13 1·-· ·3
JUMPER 14 1· · ·3
JUMPER 15 1· · ·3
JUMPER 16 1· ·-·3
JUMPER 17 1· · ·3
JUMPER 18 1· ·-·3
JUMPER 19 1· · ·3
JUMPER 20 1· · ·3
JUMPER 21 1· · ·3
JUMPER 22 1· ·-·3
JUMPER 23 1·-· ·3
JUMPER 24 1· ·-·3
JUMPER 25 1· ·-·3
JUMPER 26 1· ·-·3
JUMPER 27 1· ·-·3
JUMPER 28 1·-· ·3
JUMPER 29 1· ·-·3
JUMPER 30 1· ·-·3
JUMPER 31 1·-· ·3
JUMPER 32 1· ·-·3
JUMPER 33 1· ·-·3
JUMPER 34 1·-· ·3

LINK 1 1·-·2
LINK 2 1· ·2
LINK 3 1· ·2
LINK 4 1· ·2
LINK 5 1· ·2
LINK 6 1· ·2
LINK 7 1· ·2
LINK 8 1· ·2
LINK 9 1·-·2
LINK 10 1·-·2
LINK 11 1·-·2

LINK 12 1·-·2
LINK 13 1· ·2
LINK 14 1· ·2
LINK 15 1· ·2
LINK 16 1· ·2
LINK 17 1· ·2
LINK 18 1· ·2
LINK 19 1· ·2
LINK 20 1· ·2
LINK 21 1·-·2
LINK 22 1· ·2
LINK 23 1· ·2
LINK 24 1·-·2
LINK 25 1· ·2
LINK 26 1· ·2
LINK 27 1· ·2
LINK 28 1· ·2
LINK 29 1· ·2
LINK 30 1·-·2
LINK 31 1· ·2
LINK 32 1· ·2
LINK 33 1·-·2 (copper track - no link necessary)
LINK 34 1·-·2 (copper track - no link necessary)
LINK 35 1· ·2
LINK 36 1· ·2
LINK 37 1· ·2
LINK 38 1· ·2
LINK 39 1· ·2
LINK 40 1· ·2
LINK 41 1· ·2

3.3.17 Address maps

3.3.17.1 Flash memory (Data memory area)

2 x 32 pin JEDEC DIL sockets

	Device	Description	Size	Base address
	Am29F010×2	131,072 × 8-bit DIP	262144	$00000

3.3.17.2 Static RAM (Data memory area)

2 x 32 pin JEDEC DIL sockets

	Device	Description	Size	Base address
OR	HM628128LP×2	131,072 × 8-bit DIP	262144	$80000
OR	HM628512LP×2	524,288 × 8-bit DIP	1048576	$80000

3.3.17.3 6800 type peripherals (Data memory area)

68HC16 performs address decoding to $F0800. ADDR[10:2] coupled with FC[1:0] are decoded by PAL no PANMC3.

Device	Description	Size	Base address
G-64	VPA external address	1024	$F0800
HD63B40	Programmable timer module	8	$F0C48
HD63B40	Programmable timer module	8	$F0C50
R65C22P2	Versatile Interface Adapter	16	$F0C80

3.3.17.4 68000 type peripherals (Data memory area)

68HC16 performs address decoding to $F0000. Further de-coding of address lines A5-A10 is done by programmable logic.

XR-82C684	Quart/counter/timer, host	32	$F0420

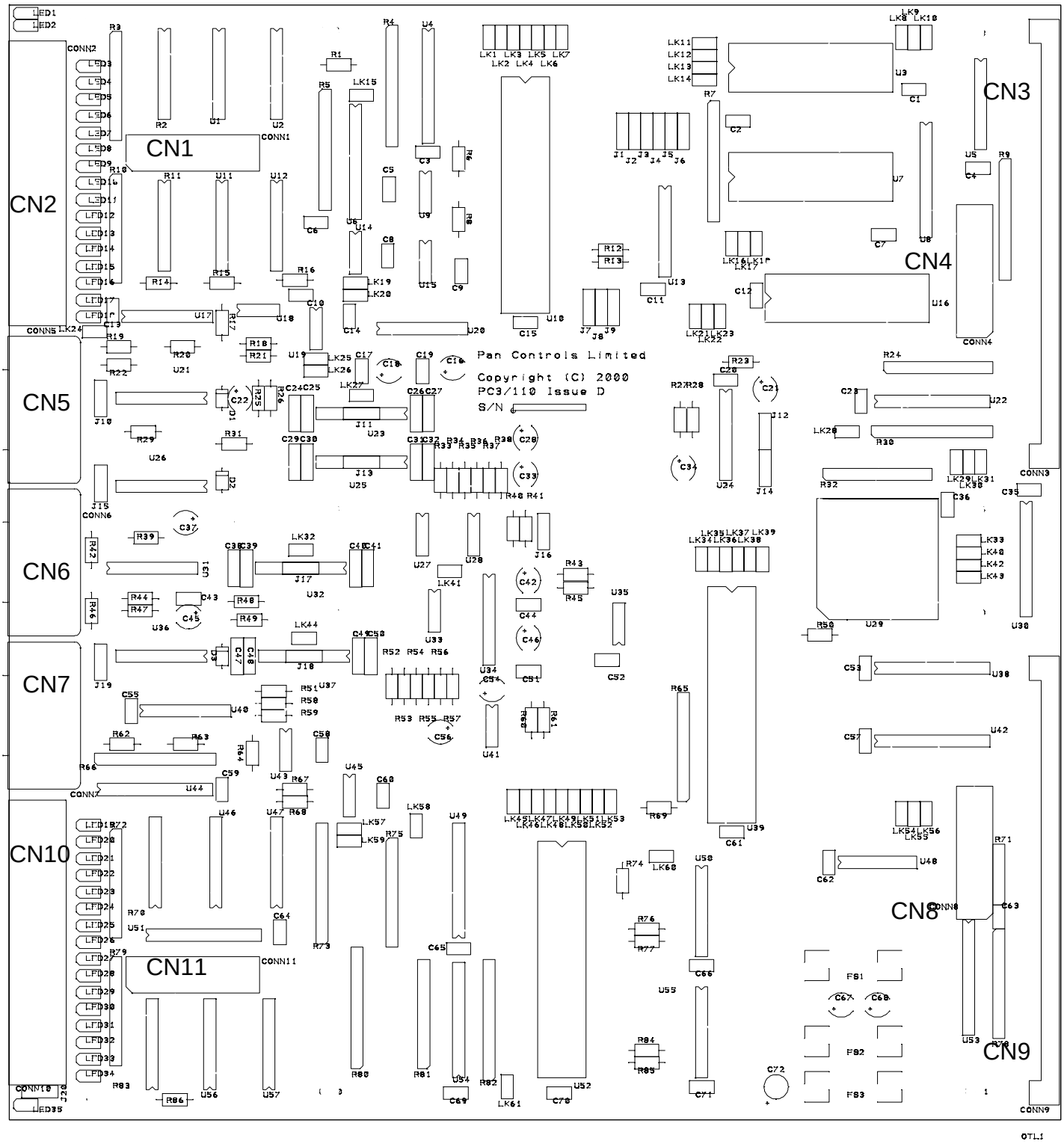
3.3.17.5 Special type peripherals (Data memory area)

68HC16 performs address decoding to $F0800. Further de-coding of address lines A5-A10 is done by programmable logic.

HCTL-2016	Quadrature decoder, host	2	$F0C00
HCTL-2016	Quadrature decoder, host	2	$F0C08

3.4 Slave Control (PC3/110) Rev D connectors & jumpers

There are eleven connectors on the board as follows:



The general arrangement is as follows:

(i) Connector 1 - 20 way header for front daughter board.
(ii) Connector 2 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated inputs.
(iii) Connector 3 - 64-way DIN 41612 type B (rows a & b). Stepper outputs & miscellaneous inputs & outputs.
(iv) Connector 4 - 20 way header for back daughter board no 1.
(v) Connector 5 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 1).
(vi) Connector 6 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 3).
(vii) Connector 7 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 2).
(viii) Connector 8 - 20 way header for back daughter board no 2.
(ix) Connector 9 - 64 way DIN 41612 type B (rows a & b). G-64 synchronous computer bus & asynchronous serial.
(x) Connector 10 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated outputs.
(xi) Connector 11 - 20 way header for front daughter board.

3.4.2 Connector 1. 20-way header for front daughter board.

1	0 volts
2	Address A0
3	Address A1
4	Address A2
5	Address A3
6	5 volts
7	N/C
8	Chip select 1
9	Chip select 2
10	Reset
11	Inverted Eclock
12	Data D0
13	Data D1
14	Data D2
15	Data D3
16	Data D4
17	Data D5
18	Data D6
19	Data D7
20	Eclock

3.4.3 Connector 2. 17 way PCB header, Klippon type SL3.5/17/90. Isolated inputs.

1	Input common (0v)
2	Input 1
3	Input 2
4	Input 3
5	Input 4
6	Input 5
7	Input 6
8	Input 7
9	Input 8
10	Input 9
11	Input 10
12	Input 11
13	Input 12
14	Input 13
15	Input 14
16	Input 15
17	Input 16

3.4.4 Connector 3. Stepper outputs. 96-way DIN 41612 type C (rows a & b).

1a	Stepper channel 1 clock
1b	Stepper channel 1 direction
2a	Stepper channel 2 clock
2b	Stepper channel 2 direction
3a	Stepper channel 3 clock
3b	Stepper channel 3 direction
4a	Stepper channel 4 clock
4b	Stepper channel 4 direction
5a	N/C
5b	
6a	
6b	
7a	
7b	
8a	
8b	0V
9a	
9b	0V
10a	
10b	0V
11a	
11b	0V
12a	
12b	0V
13a	0V
13b	0V
14a	
14b	0V
15a	
15b	0V
16a	
16b	0V
17a	
17b	0V
18a	
18b	0V
19a	

19b 0V
20a
20b 0V
21a Pin 9 of 75245 (U22) buffer
21b 0V
22a N/C
22b N/C
23a N/C
23b N/C
24a N/C
24b N/C
25a N/C
25b N/C
26a N/C
26b N/C
27a N/C
27b N/C
28a N/C
28b N/C
29a N/C
29b N/C
30a N/C
30b N/C
31a N/C
31b N/C
32a N/C
32b N/C

3.4.5 Connector 4. 20-way header for daughter board.

1 0 volts
2
3
4
5
6 5 volts
7
8
9
10
11 IRQD1
12 MC68HC16 MOSI (Tx Synchronous port)
13 MC68HC16 MISO (Rx Synchronous port)
14 MC68HC16 SCK (CLK Synchronous port)
15 MC68HC16 /RESET
16 MC68HC16 PCS1 (Synchronous port chip select)
17 MC68HC16 PCS0 (Synchronous port chip select)
18 MC68HC16 PCS2 (Synchronous port chip select)
19 MC68HC16 PCS3 (Synchronous port chip select)
20 MC68HC16 ECLOCK

3.4.6 Connector 5. Position encoder, reference i/p, analogue o/p.

1 Ch.1 encoder track A
2 Ch.1 encoder track $\overline{A}$
3 Ch.1 encoder track B
4 Ch.1 encoder track $\overline{B}$
5 Ch.1 encoder track Z
6 Ch.1 velocity isolated supply (+15v) VR1
7 Ch.1 velocity isolated supply (-15v) VT1
8 Ch.1 encoder power supply 0v EVS1
9 Ch.1 encoder power supply +ve EVR1
10 Ch.1 encoder track $\overline{Z}$
11 Ch.1 velocity signal (DAC port A) AVEL
12 Ch.1 DAC aux. output (DAC port C) CAUX
13 Ch.1 velocity isolated supply 0v VS1
14 Ch.1 Relay Common 1COM
15 Ch.1 Relay normally open or normally closed (jumper selectable) 1CON

3.4.7 Connector 6. Position encoder, reference i/p, analogue o/p.

1 Ch.3 encoder track A
2 Ch.3 encoder track $\overline{A}$
3 Ch.3 encoder track B
4 Ch.3 encoder track $\overline{B}$
5 Ch.3 encoder track Z
6 Ch.3 velocity isolated supply (+15v) VR3
7 Ch.3 velocity isolated supply (-15v) VT3
8 Ch.3 encoder power supply 0v EVS3
9 Ch.3 encoder power supply +ve EVR3
10 Ch.3 encoder track $\overline{Z}$
11 Ch.3 velocity signal (DAC port A) AVEL
12
13 Ch.3 velocity isolated supply 0v VS3
14 Ch.3 Relay Common 1COM
15 Ch.3 Relay normally open or normally closed (jumper selectable) 1CON

3.4.8 Connector 7. Position encoder, reference i/p, analogue o/p.

1 Ch.2 encoder track A
2 Ch.2 encoder track $\overline{A}$
3 Ch.2 encoder track B
4 Ch.2 encoder track $\overline{B}$
5 Ch.2 encoder track Z
6 Ch.2 velocity isolated supply (+15v) VR2
7 Ch.2 velocity isolated supply (-15v) VT2
8 Ch.2 encoder power supply 0v EVS2
9 Ch.2 encoder power supply +ve EVR2
10 Ch.2 encoder track $\overline{Z}$
11 Ch.2 velocity signal (DAC port A) AVEL
12
13 Ch.2 velocity isolated supply 0v VS2
14 Ch.2 Relay Common 1COM
15 Ch.2 Relay normally open or normally closed (jumper selectable) 1CON

3.4.9 Connector 8. 20-way header for daughter board.

1	0 volts
2	
3	
4	
5	
6	5 volts
7	
8	
9	
10	
11	IRQD1
12	MC68HC16 MOSI (Tx Synchronous port)
13	MC68HC16 MISO (Rx Synchronous port)
14	MC68HC16 SCK (CLK Synchronous port)
15	MC68HC16 /RESET
16	MC68HC16 PCS1 (Synchronous port chip select)
17	MC68HC16 PCS0 (Synchronous port chip select)
18	MC68HC16 PCS2 (Synchronous port chip select)
19	MC68HC16 PCS3 (Synchronous port chip select)
20	MC68HC16 ECLOCK

3.4.10 Connector 9

G-64 bus signals and functions

Details of the G-64 bus signals and their functions are shown below. A '/' prefix on the signal name denotes an active low signal. A '*' in the "Used" column indicates the signals which are used on this board. A '**' indicates that the signals are used and that they differ from the G-64 standard.

Pin	Signal	I/O	Used	Function
1a	GND	O	✶	0V supply
1b	GND	O	✶	0V supply
2a	A0	O	✶	Address bit 0 (least significant) Address outputs from processor board.
2b	A8	O	✶	Address bit 8
3a	A1	O	✶	Address bit 1
3b	A9	O	✶	Address bit 9
4a	A2	O	✶	Address bit 2
4b	$\overline{PCS0}$	O	✶✶	SPI chip select 0 The SPI chip selects can be decoded to provide 15 individual chip selects.
5a	A3	O	✶	Address bit 3
5b	$\overline{PCS1}$	O	✶✶	SPI chip select 1
6a	A4	O	✶	Address bit 4
6b	$\overline{PCS2}$	O	✶✶	SPI chip select 2
7a	A5	O	✶	Address bit 5
7b	$\overline{PCS3}$	O	✶✶	SPI chip select 3
8a	A6	O	✶	Address bit 6
8b	SCK	O	✶✶	SPI synchronous clock
9a	A7	O	✶	Address bit 7
9b	MOSI	O	✶✶	SPI Master Out Slave In
10a	$\overline{BGRT}$	O		Bus Grant
10b	$\overline{BRQ}$	I		Bus Request
11a	$\overline{REFGNT}$	I/O		Refresh cycle grant
11b	$\overline{REFREQ}$	I/O		Refresh cycle request
12a	$\overline{HALT}$	I/O		Halt processor
12b	$\overline{BGACK}$	I/O		Bus Grant Acknowledge
13a2		SYS	O	System clock
13b	ECLOCK	O	✶	E clock Data transfer takes place when E is high
14a	$\overline{VPA}$	O	✶	Valid Peripheral Address
14b	$\overline{RES}$	O	✶	System Reset signal

Pin	Signal	I/O	Used	Function
15a	DTACK	I/O	✶	Data Transfer Acknowledge signal.
15b	NMI	I	✶	Non-Maskable Interrupt
16a	AS	O		Address Strobe
16b	IRQ	O	✶	Interrupt Request
17a	R/W	O	✶	Read/Write.
17b	FIRQ	I/O	✶	Fast Interrupt Request
18a	HALTACK	O		Halt Acknowledge
18b	IACK	O		Interrupt Acknowledge
19a	D8	I/O		Data bit 8.
19b	D12	I/O		Data bit 12.
20a	D9	I/O		Data bit 9.
20b	D13	I/O		Data bit 13.
21a	D10	I/O		Data bit 10.
21b	D14	I/O		Data bit 14.
22a	D11	I/O		Data bit 11.
22b	D15	I/O		Data bit 15 (most significant).
23a	D0	I/O	✶	Data bit 0 (least significant).
23b	D4	I/O	✶	Data bit 4.
24a	D1	I/O	✶	Data bit 1.
24b	D5	I/O	✶	Data bit 5.
25a	D2	I/O	✶	Data bit 2.
25b	D6	I/O	✶	Data bit 6.
26a	D3	I/O	✶	Data bit 3.
26b	D7	I/O	✶	Data bit 7.
27a	MISO	I	✶✶	SPI Master In Slave Out
27b	PERR	I		Parity Error/ Bus Error
28a	CH.OUT	O		Daisy chain output
28b	CH.IN	I		Daisy chain input
29a	-5V	I		-5V supply
29b	+5V BAT	I		+5v supply from standby battery
30a	+15V	I	✶✶	+15V supply
30b	-15V	I	✶✶	-15V supply
31a	+5V	I	✶	+5V supply
31b	+5V	I	✶	+5V supply
32a	GND	I	✶	0V supply
32b	GND	I	✶	0V supply

3.4.11 Connector 10. 17 way PCB header, Klippon type SL3.5/17/90. Isolated outputs.

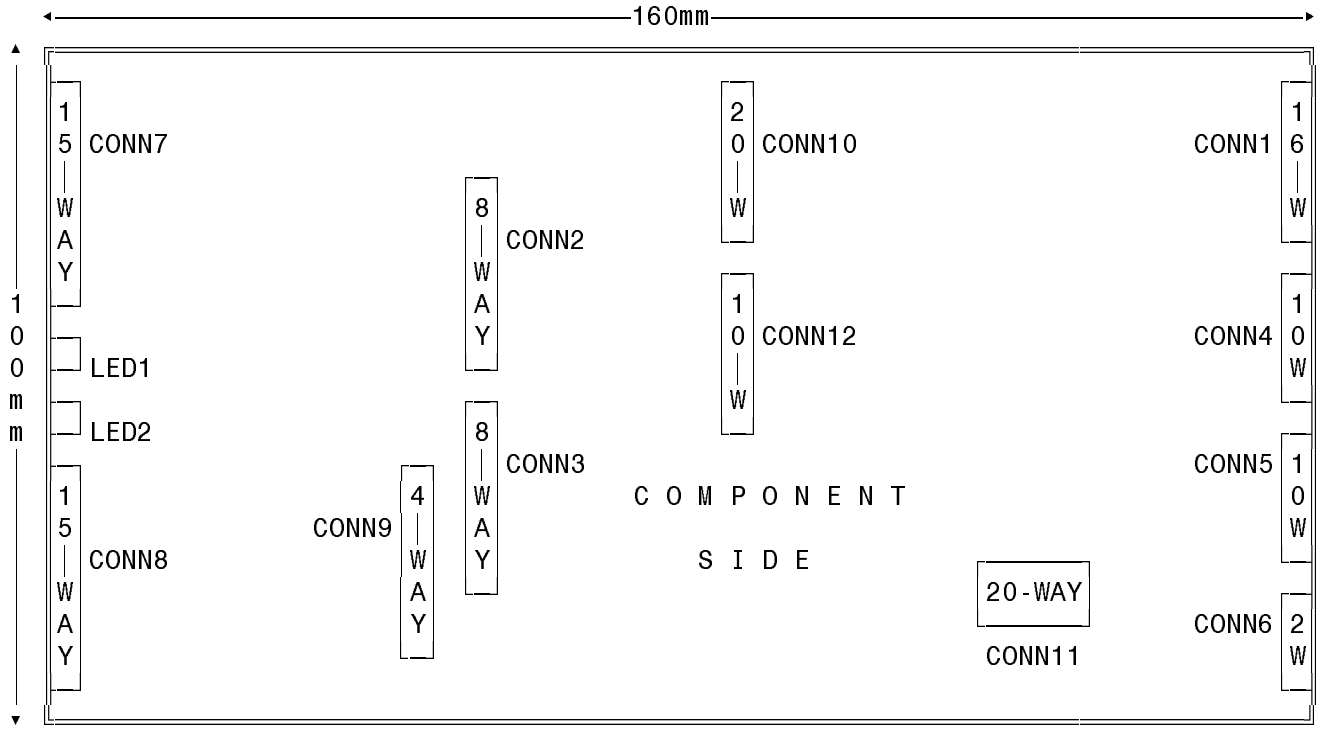
1	Output common (24v DC)
2	Output 1
3	Output 2
4	Output 3
5	Output 4
6	Output 5
7	Output 6
8	Output 7
9	Output 8
10	Output 9
11	Output 10
12	Output 11
13	Output 12
14	Output 13
15	Output 14
16	Output 15
17	Output 16

3.4.12 Connector 11. 20-way header for front daughter board.

1	0 volts
2	CA2 IRQ i/p on U39 (6821)
3	+15v
4	-15v
5	0 volts analogue
6	5 volts
7	CB1 IRQ i/p on U52 (6821)
8	CB2 IRQ i/p on U52 (6821)
9	Address A4
10	Chip select 1
11	IRQ
12	MOSI
13	MISO
14	SCK
15	Chip select 2
16	SPCS0
17	SPCS1
18	SPCS2
19	SPCS3
20	CA2 IRQ i/p on U52 (6821)

3.5 Operator interface (PC3/120) connectors & jumpers

The general arrangement is as follows:



The height of the board is 'Eurocard' size (100mm).

There are twelve connectors on the board as follows:

(i) Connector 1 - 16 way header for VFD/LCD display.
(ii) Connector 2 - 8 way header for keypad.
(iii) Connector 3 - 8 way header for keypad.
(iv) Connector 4 - 10 way header for serial comms.
(v) Connector 5 - 10 way header for serial IR comms.
(vi) Connector 6 - 2 way header for power supply.
(vii) Connector 7 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 1).
(viii) Connector 8 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 2).
(ix) Connector 9 - 4 way header for analogue power supply.
(x) Connector 10 - 20 way header for parallel peripherals.
(xi) Connector 11 - 20 way header for parallel i/o.
(xii) Connector 12 - 10 way header for serial peripherals.

3.5.2 Connector 1. 16 way header for VFD/LCD display.

1	0 volts DC
2	+5 volts DC
3	Variable power supply for LCD
4	Address 0
5	R/W
6	E clock
7	Data 0
8	Data 1
9	Data 2
10	Data 3
11	Data 4
12	Data 5
13	Data 6
14	Data 7
15	Chip select
16	Reset

3.5.3 Connector 2. 8 way header for keypad.

1	Scan input from keypad no 1
2	Scan input from keypad no 2
3	Scan input from keypad no 3
4	Scan input from keypad no 4
5	Scan input from keypad no 5
6	Scan input from keypad no 6
7	Scan input from keypad no 7
8	Scan input from keypad no 8

3.5.4 Connector 3. 8 way header for keypad.

1	Scan output to keypad no 1
2	Scan output to keypad no 2
3	Scan output to keypad no 3
4	Scan output to keypad no 4
5	Scan output to keypad no 5
6	Scan output to keypad no 6
7	Scan output to keypad no 7
8	Scan output to keypad no 8

3.5.5 Connector 4. 10 way header for serial comms.

1	Unregulated DC power supply input (6.5-9 volts DC)
2	Unregulated DC power supply input (6.5-9 volts DC)
3	RS-232 channel 1 transmit or RS-422 (A) channel 1 receive
4	RS-232 channel 2 receive or RS-422 (B) channel 1 receive
5	RS-232 channel 1 receive or RS-422 (B) channel 1 transmit
6	RS-232 channel 2 transmit orRS-422 (A) channel 1 transmit
7	No connection
8	0 volts DC
9	0 volts DC
10	No connection

3.5.6 Connector 5. 10 way header for serial IR comms.

1 16 × clock
2 No connection
3 Channel 1 receive
4 No connection
5 0 volts DC
6 0 volts DC
7 Channel 1 transmit
8 0 volts DC
9 5 volts DC
10 5 volts DC

3.5.7 Connector 6. 2 way header for power supply.

1 Unregulated DC power supply input (6.5-9 volts DC)
2 0 volts DC

3.5.8 Connector 7. 15-way D connector, for position encoder, reference i/p, analogue o/p.

1 Ch.1 encoder track A
2 Ch.1 encoder track $\overline{A}$
3 Ch.1 encoder track B
4 Ch.1 encoder track $\overline{B}$
5 Ch.1 encoder track Z
6 No connection
7 No connection
8 Ch.1 encoder power supply 0v *EVS1*
9 Ch.1 encoder power supply +ve *EVR1*
10 Ch.1 encoder track $\overline{Z}$
11 Ch.1 velocity signal (DAC port B) *AVEL*
12 No connection
13 Ch.1 velocity 0v (analogue ground) *VS1*
14 Ch.1 Relay Common *1COM*
15 Ch.1 Relay normally open or normally closed (jumper selectable) *1CON*

3.5.9 Connector 8. 15-way D connector, for position encoder, reference i/p, analogue o/p.

1 Ch.2 encoder track A
2 Ch.2 encoder track $\overline{A}$
3 Ch.2 encoder track B
4 Ch.2 encoder track $\overline{B}$
5 Ch.2 encoder track Z
6 No connection
7 No connection
8 Ch.2 encoder power supply 0v *EVS2*
9 Ch.2 encoder power supply +ve *EVR2*
10 Ch.2 encoder track $\overline{Z}$
11 Ch.2 velocity signal (DAC port B) *BVEL*
12 No connection
13 Ch.2 velocity 0v (analogue ground) *VS2*
14 Ch.2 Relay Common *2COM*
15 Ch.2 Relay normally open or normally closed (jumper selectable) *2CON*

3.5.10 Connector 9. 4 way header for analogue power supply.

1	Analogue Ground
2	Analogue Ground
3	-15 volts DC (regulated)
4	+15 volts DC (regulated)

3.5.11 Connector 10. 20 way header for parallel peripherals.

1	0 volts DC
2	MC68HC11 address A0
3	MC68HC11 address A1
4	MC68HC11 address A2
5	MC68HC11 address A3
6	+5 volts DC
7	MC68HC11 address R/W
8	Chip select 1
9	Chip select 2
10	Reset
11	ŧRQ
12	MC68HC11 data D0
13	MC68HC11 data D1
14	MC68HC11 data D2
15	MC68HC11 data D3
16	MC68HC11 data D4
17	MC68HC11 data D5
18	MC68HC11 data D6
19	MC68HC11 data D7
20	MC68HC11 data E clock

3.5.12 Connector 11. 20 way header for parallel i/o.

1	0 volts DC	
2	+5 volts DC	
3	MC68B21 (PIA) PB0	Input no 1
4	MC68B21 (PIA) PA0	
5	MC68B21 (PIA) PB1	Input no 2
6	MC68B21 (PIA) PA1	
7	MC68B21 (PIA) PB2	Input no 3
8	MC68B21 (PIA) PA2	
9	MC68B21 (PIA) PB3	Input no 4
10	MC68B21 (PIA) PA3	
11	MC68B21 (PIA) PB4 (Line driver output)	Output no 1
12	MC68B21 (PIA) PA4	
13	MC68B21 (PIA) PB5 (Line driver output)	Output no 2
14	MC68B21 (PIA) PA5	
15	MC68B21 (PIA) PB6 (Line driver output)	Output no 3
16	MC68B21 (PIA) PA6	
17	MC68B21 (PIA) PB7 (Line driver output)	Output no 4
18	MC68B21 (PIA) PA7	
19	0 volts DC	
20	+5 volts DC	

3.5.13 Connector 12. 10 way header for serial peripherals.

1	MC68HC11 MOSI
2	MC68HC11 SCK
3	MC68HC11 MISO
4	MC68HC11 PG0
5	MC68HC11 PG1
6	MC68HC11 PG2
7	0 volts DC
8	+5 volts DC
9	MC68HC11 PG3
10	ŧRQ

3.5.14 Jumpers.

Jumper	Function	Connections
2	0v to pin 4 of U6 (RS485 direction control)	1-2
	Pin 3 of Jumper 11 to pin 4 of U6 (RS485 direction control)	2-3
3	Pin 18(XŧRQ) of U1 (68HC11) to pin 38 (ŧRQA) of U14 (PIA)	1-2
	Pin 19(ŧRQ) of U1 (68HC11) to pin 38 (ŧRQA) of U14 (PIA)	2-3
4	Pin 18(XŧRQ) of U1 (68HC11) to pin 37 (ŧRQB) of U14 (PIA)	1-2
	Pin 19(ŧRQ) of U1 (68HC11) to pin 37 (ŧRQB) of U14 (PIA)	2-3
5	Pin 18(XŧRQ) of U1 (68HC11) to pin 11 of connector 10	1-2
	Pin 19(ŧRQ) of U1 (68HC11) to pin 11 of connector 10	2-3
7	Relay N/C (ch1) to pin 15 of conn 7	1-2
	Relay N/O (ch1) to pin 15 of conn 7	2-3
8	Watchdog OK Relay enable (DAC)	2-3
	0v to Relay enable (DAC)	1-2
9	Watchdog OK Relay enable (PG5)	2-3
	0v to Relay enable (PG5)	1-2
10	Pin 42(PA0) of U1 (68HC11) to pin 6 of U26 (relay 2 control)	1-2
	Pin 42(PA0) of U1 (68HC11) to pin 9 of U5 (Channel 1 Rxd)	2-3
11	Pin 39(PA3) of U1 (68HC11) to pin 1 of U26 (relay 1 control)	1-2
	Pin 39(PA3) of U1 (68HC11) to pin 10 of U5 (Channel 1 Txd)	2-3
18	Pin 18(XŧRQ) of U1 (68HC11) to pin 10 of connector 12	1-2
	Pin 19(ŧRQ) of U1 (68HC11) to pin 10 of connector 12	2-3
19	Relay N/C (ch2) to pin 15 of conn 8	1-2
	Relay N/O (ch2) to pin 15 of conn 8	2-3
20	Pin 44(PB6) of U1 (68HC11) to pin 27 (A14) of U3 (EPROM)	1-2
	Pin 5(RW) of U1 (68HC11) to pin 27 (A14) of U3 (EPROM)	1-2
21	Pin 43(PB7) of U1 (68HC11) to pin 1 (A15) of U3 (EPROM)	1-2
	Pin 44(PB6) of U1 (68HC11) to pin 1 (A15) of U3 (EPROM)	1-2

3.5.15 Link definitions.

Link	Function	Connections
1	Pin 29(PD1) of U1 (68HC11) to pin 11(T1IN) of U5 (MAX 232)	1-2
2	Pin 28(PD0) of U1 (68HC11) to pin 12(R1OUT) of U5 (MAX 232)	1-2
3	Pin 2(MODB) of U1 (68HC11) to 0 volts DC	1-2
4	Pin 3(MODA) of U1 (68HC11) to 0 volts DC	1-2
5	Pin 28(PD0) of U1 (68HC11) to Pin 18(XIRQ) of U1 (68HC11)	1-2
6	Pin 3(WP) of U9 (X25040) to 0 volts DC	1-2
7	Pin 5(2Y) of U17 (AM26LS33) to Pin 39(CA2) of U14 (PIA)	1-2
8	Pins 1(GBA) & 13(GAB) of U15 (74HC243) to 0 volts DC	1-2

3.5.16 Default jumper settings.

This shows the default settings for the jumpers for an operator interface board:

PC3/120 (Operator interface)

```
JUMPER 1     · ·
JUMPER 2     · ·
JUMPER 3     · ·
JUMPER 4     ·-·
JUMPER 7    1· ·-·3
JUMPER 9    1· ·-·3
JUMPER 10   1· ·-·3
JUMPER 11   1· ·-·3

LINK 1    1·-·2
LINK 2    1· ·2
```


3.6 Address maps for PC3/120 board

3.6.1 EPROM

1 x 28 pin JEDEC DIL socket

Device	Description	Size	Base address	Chip select
M27C512×1	65,536 x 8-bit DIP	65536	$0000	CSPRG (PG7)

3.6.2 Static RAM

1 x 28 pin JEDEC DIL socket

Device	Description	Size	Base address	Chip select
HM62256ALP×1	32,768 × 8-bit DIP	32768	$0000	CSGEN (PG6)

3.6.3 Versatile Interface Adaptor (VIA)

Device	Description	Size	Base address	Chip select
R65C21	Peripheral Interface Adaptor	4	$1C00	CSIO1 (PG5)

3.6.4 Quadrature decoder & counter

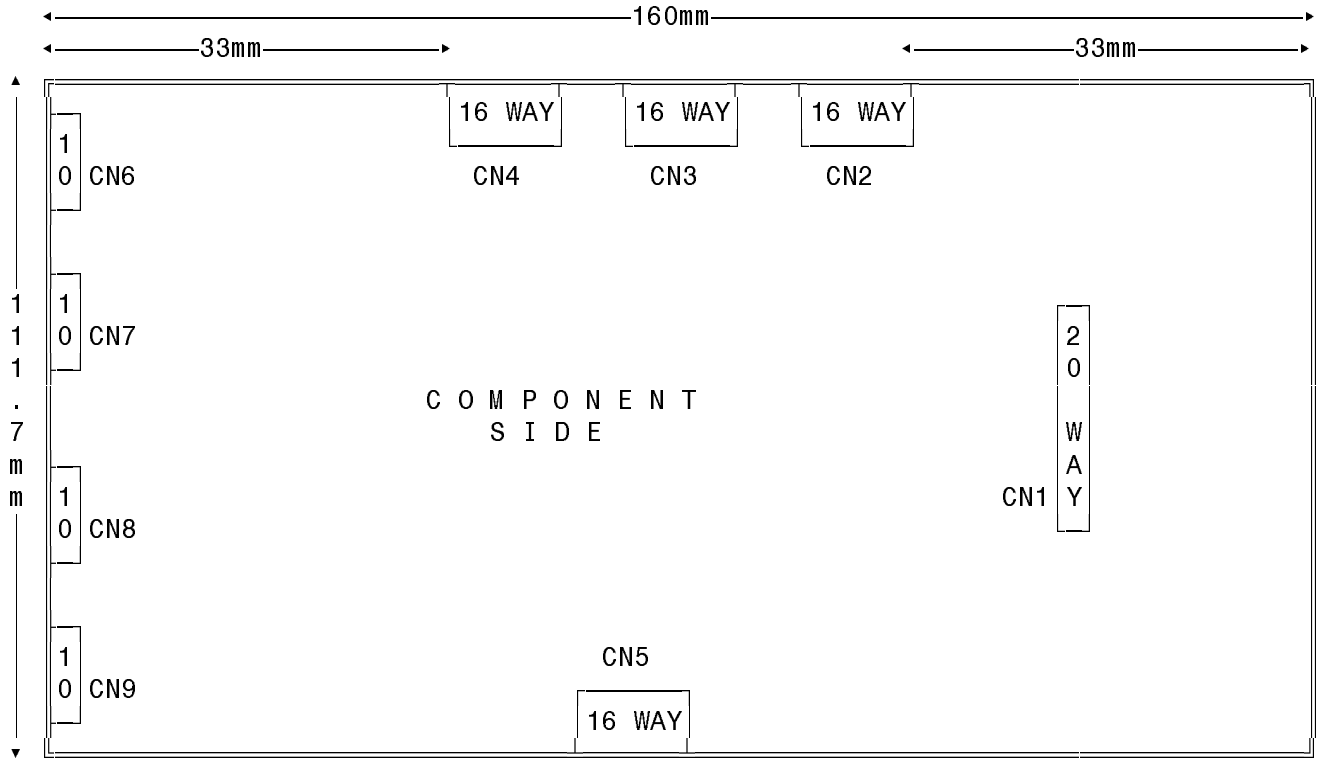
Device	Description	Size	Base address	Chip select
HCTL-2016	Quadrature decoder	2	$1C10	CSIO1 (PG5)

3.6.5 G-64 bus

Device	Description	Size	Base address	Chip select
G-64	VPA external address	1024	$1800	CSIO1 (PG5)

3.7 Daughter board (PC3/130) connectors & jumpers

The general arrangement is as follows:



The height of the board is 'Module' size (111.7mm).

There are nine connectors on the board as follows:

(i) Connector 1 - 20 way header for control board.
(ii) Connector 2 - 16 way header for L.E.D. displays.
(iii) Connector 3 - 16 way header for L.E.D. displays.
(iv) Connector 4 - 16 way header for L.E.D. displays.
(v) Connector 5 - 16 way header for L.E.D. displays.
(vi) Connector 6 - 10 way header for RS-422 communications.
(vii) Connector 7 - 10 way header for RS-422 communications.
(viii) Connector 8 - 10 way header for RS-422 communications.
(ix) Connector 9 - 10 way header for RS-422 communications.

3.7.2 Connector 1. 20-way header for control board.

1	0 volts
2	TXDA (Tx Asynchronous port 1)
3	RXDA (Rx Asynchronous port 1)
4	TXDB (Tx Asynchronous port 2)
5	RXDB (Rx Asynchronous port 2)
6	5 volts
7	TXDC (Tx Asynchronous port 3)
8	RXDC (Rx Asynchronous port 3)
9	TXDD (Tx Asynchronous port 4)
10	RXDD (Rx Asynchronous port 4)
11	Spare
12	MOSI (Tx Synchronous port)
13	MISO (Rx Synchronous port)
14	SCK (CLK Synchronous port)
15	Spare
16	PCS1 (Synchronous port chip select)
17	PCS0 (Synchronous port chip select)
18	PCS2 (Synchronous port chip select)
19	PCS3 (Synchronous port chip select)
20	ECLOCK

3.7.3 Connector 2. 16 way header for L.E.D. displays.

1	Segment A
2	Segment D
3	Common cathode, digit 1
4	Common cathode, digit 2
5	Segment C
6	Common cathode, digit 3
7	Segment B
8	Segment F
9	Segment E
10	Common cathode, digit 4
11	Segment DP
12	Segment G
13	Common cathode, digit 5
14	Common cathode, digit 6
15	Common cathode, digit 7
16	Common cathode, digit 8

3.7.4 Connector 3. 16 way header for L.E.D. displays.

1	Segment A
2	Segment D
3	Common cathode, digit 1
4	Common cathode, digit 2
5	Segment C
6	Common cathode, digit 3
7	Segment B
8	Segment F
9	Segment E
10	Common cathode, digit 4
11	Segment DP
12	Segment G
13	Common cathode, digit 5
14	Common cathode, digit 6
15	Common cathode, digit 7
16	Common cathode, digit 8

3.7.5 Connector 4. 16 way header for L.E.D. displays.

1	Segment A
2	Segment D
3	Common cathode, digit 1
4	Common cathode, digit 2
5	Segment C
6	Common cathode, digit 3
7	Segment B
8	Segment F
9	Segment E
10	Common cathode, digit 4
11	Segment DP
12	Segment G
13	Common cathode, digit 5
14	Common cathode, digit 6
15	Common cathode, digit 7
16	Common cathode, digit 8

3.7.6 Connector 5. 16 way header for L.E.D. displays.

1	Segment A
2	Segment D
3	Common cathode, digit 1
4	Common cathode, digit 2
5	Segment C
6	Common cathode, digit 3
7	Segment B
8	Segment F
9	Segment E
10	Common cathode, digit 4
11	Segment DP
12	Segment G
13	Common cathode, digit 5
14	Common cathode, digit 6
15	Common cathode, digit 7
16	Common cathode, digit 8

3.7.7 Connector 6. 10 way header for RS-422 communications.

1	0v isolated
2	+5v isolated (optional via jumper)
3	Tx-transmitted data
4	/Tx-transmitted data complement
5	Rx-received data
6	/Rx-received data complement
7	Spare
8	Spare
9	Spare
10	Spare

3.7.8 Connector 7. 10 way header for RS-422 communications.

1	0v isolated
2	+5v isolated (optional via jumper)
3	Tx-transmitted data
4	/Tx-transmitted data complement
5	Rx-received data
6	/Rx-received data complement
7	Spare
8	Spare
9	Spare
10	Spare

3.7.9 Connector 8. 10 way header for RS-422 communications.

1	0v isolated
2	+5v isolated (optional via jumper)
3	Tx-transmitted data
4	/Tx-transmitted data complement
5	Rx-received data
6	/Rx-received data complement
7	Spare
8	Spare
9	Spare
10	Spare

3.7.10 Connector 9. 10 way header for RS-422 communications.

1	0v isolated
2	+5v isolated (optional via jumper)
3	Tx-transmitted data
4	/Tx-transmitted data complement
5	Rx-received data
6	/Rx-received data complement
7	Spare
8	Spare
9	Spare
10	Spare

3.7.11 Jumpers.

Jumper	Function	Connections	
1 (3 pins)	MAX7219 no 2 Din to MAX7219 no 1 Dout		1-2
	MAX7219 no 2 Din to PANMC10 pin 18	2-3	
2 (3 pins)	MAX7219 no 3 Din to MAX7219 no 2 Dout		1-2
	MAX7219 no 3 Din to PANMC10 pin 18	2-3	
3 (3 pins)	MAX7219 no 4 Din to MAX7219 no 3 Dout		1-2
	MAX7219 no 4 Din to PANMC10 pin 18	2-3	
4 (2 pins)	PANMC10 pin 8 to GND (else pulled high)	1-2	
5 (2 pins)	PANMC10 pin 9 to GND (else pulled high)	1-2	
6 (2 pins)	PANMC10 pin 11 to GND (else pulled high)	1-2	
7 (2 pins)	Isolated 5v (channel 1) to connector 6 pin2	1-2	
8 (2 pins)	Isolated 5v (channel 2) to connector 7 pin2	1-2	
9 (2 pins)	Isolated 5v (channel 3) to connector 8 pin2	1-2	
10 (2 pins)	Isolated 5v (channel 4) to connector 9 pin2	1-2	
11 (3 pins)	Channel 1 Rxd to connector 1 pin 3	1-2	
	Channel 1 Rxd to connector 1 pin 13	2-3	
12 (3 pins)	Channel 1 Txd to connector 1 pin 2	1-2	
	Channel 1 Txd to PANMC10 pin 18	2-3	
13 (3 pins)	Channel 2 Txd to connector 1 pin 4	1-2	
	Channel 2 Txd to PANMC10 pin 19	2-3	
14 (3 pins)	Channel 3 Txd to connector 1 pin 7	1-2	
	Channel 3 Txd to PANMC10 pin 14	2-3	
15 (3 pins)	Channel 4 Txd to connector 1 pin 9	1-2	
	Channel 4 Txd to PANMC10 pin 15	2-3	

3.7.12 Jumper settings - PC3/130 daughter boards.

This shows the default settings for the jumpers for a daughter board:

PC3/130 (Daughter)

```
JUMPER 1   1· ·-·3
JUMPER 2   1· ·-·3
JUMPER 3   1· ·-·3
JUMPER 4   1·-· ·3
JUMPER 5   1·-· ·3
JUMPER 6   1·-· ·3
JUMPER 7   1·-· ·3

LINK 1     · ·
LINK 2     · ·
LINK 3     · ·
LINK 4     · ·
LINK 5     · ·
LINK 6     ·-·
LINK 7     · ·
```

3.7.13 RS-422 cable connections.

Connections for cable between daughter board (PC3/130) and 9-pin D socket:

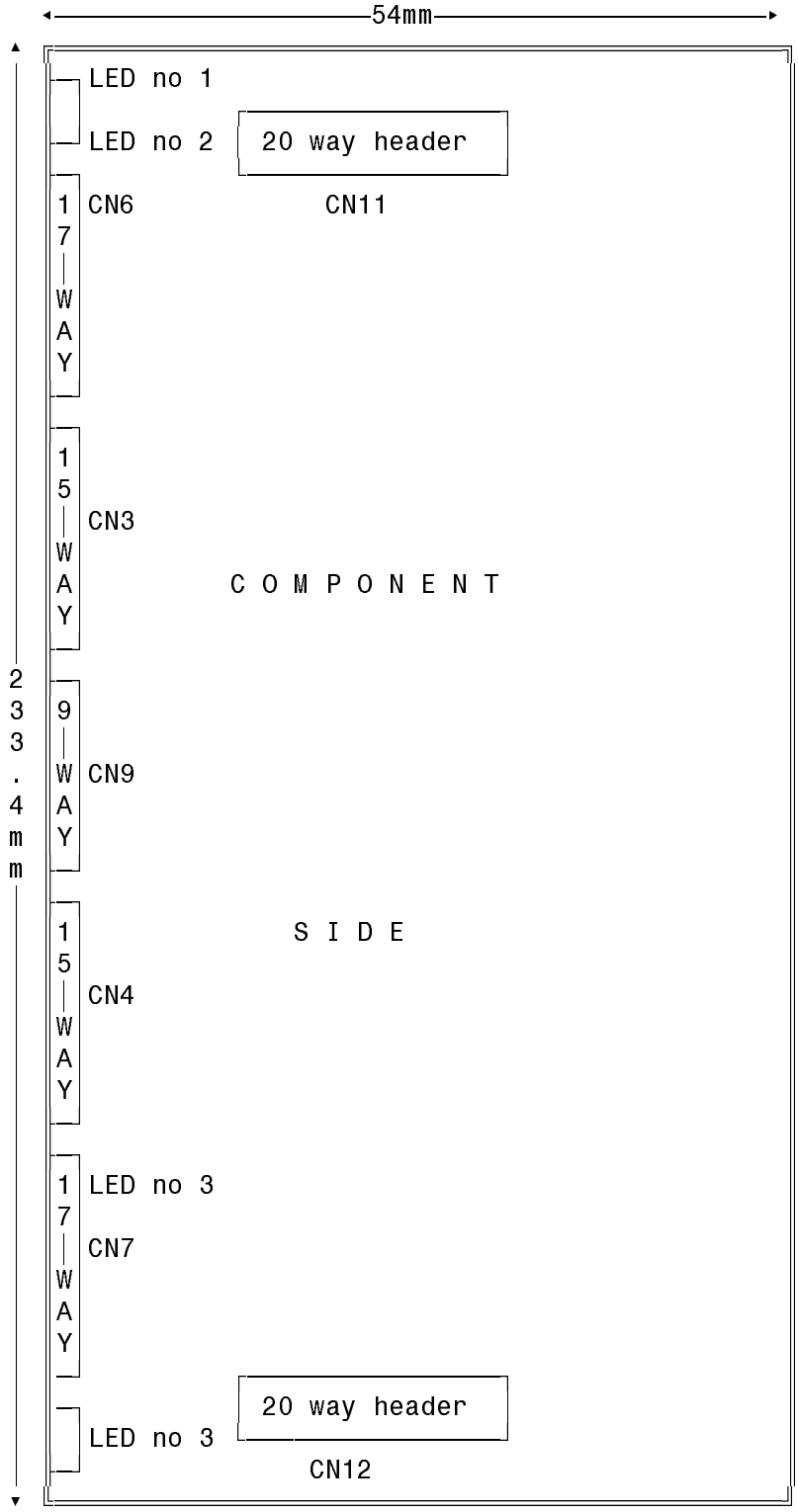
10-pin header(PC3/130)	Function	9-pin D socket
1	0v isolated o/p	1
2	+5v isolated o/p	6
3	Tx	2
4	/Tx	7
5	Rx	3
6	/Rx	8

Connections for cable between 2 daughter boards (PC3/130):

9-pin D plug	9-pin D plug
1	1
2	8
3	7
7	3
8	2

3.8 Auxiliary control board (PC3/135) connectors & jumpers

There are fifteen connectors on the board as follows:



The height of the board is double Eurocard size (233.4mm).

The general arrangement is as follows:

(i) Connector 1 - 20 way header for daughter board no 1.
(ii) Connector 2 - 20 way header for daughter board no 2.
(iii) Connector 3 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 1).
(iv) Connector 4 - 15-way D connector, for position encoder, reference signals, and analogue outputs (channel 2).
(v) Connector 5 - 64 way DIN 41612 type B (rows a & b). G-64 synchronous computer bus & asynchronous serial.
(vi) Connector 6 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated inputs.
(vii) Connector 7 - 17 way PCB header, Klippon type SL3.5/17/90. Isolated outputs.
(viii) Connector 8 - 64-way DIN 41612 type C (rows a & c). Isolated analogue inputs & timer inputs & outputs.
(ix) Connector 9 - 9-way D connector, for RS-232 serial connections.
(x) Connector 10 - 10 way header, for background mode debugging.
(xi) Connector 11 - 20 way header for front daughter board.
(xii) Connector 12 - 20 way header for front daughter board.
(xiii) Connector 13 - 10-way header, for RS-485 & Canbus.
(xiv) Connector 14. 20-way header for LCD display.
(xv) Connector 15. 20-way SIL header for keypad

3.8.2 Connector 1. 20-way header for daughter board.

1 0 volts
2 XR-82C684 TXDA (Tx Asynchronous port 1)
3 XR-82C684 RXDA (Rx Asynchronous port 1)
4 XR-82C684 TXDB (Tx Asynchronous port 2)
5 XR-82C684 RXDB (Rx Asynchronous port 2)
6 5 volts
7 XR-82C684 TXDC (Tx Asynchronous port 3)
8 XR-82C684 RXDC (Rx Asynchronous port 3)
9 MC68HC16 TXD (Tx Asynchronous port 4)
10 MC68HC16 RXD (Rx Asynchronous port 4)
11 IRQD2
12 MC68HC16 MOSI (Tx Synchronous port)
13 MC68HC16 MISO (Rx Synchronous port)
14 MC68HC16 SCK (CLK Synchronous port)
15 MC68HC16 /RESET
16 MC68HC16 PCS1 (Synchronous port chip select)
17 MC68HC16 PCS0 (Synchronous port chip select)
18 MC68HC16 PCS2 (Synchronous port chip select)
19 MC68HC16 PCS3 (Synchronous port chip select)
20 MC68HC16 ECLOCK

3.9 TIO33 board connectors & jumpers

Pin no	Row a function	Direction	Chip detail	Row c function	Direction	Chip detail
1	Ground			Global zero volt	Input	See below **(*)**
2	Ground			Channel 1	Input	PTM_05 - C2
3	Ground			Channel 2	Input	PTM_05 - C3
4	Ground			Channel 3	Input	PTM_06 - C1
5	Ground			Channel 4	Input	PTM_06 - C2
6	Ground			Channel 5	Input	PTM_06 - C3
7	Ground			Channel 6	Input	PTM_07 - C1
8	Ground			Channel 7	Input	PTM_07 - C2
9	Ground			Channel 8	Input	PTM_07 - C3
10	Ground			Channel 9	Input	PTM_08 - C1
11	Ground			Channel 10	Input	PTM_08 - C2
12	Ground			Channel 11	Input	PTM_08 - C3
13	Ground			Channel 12	Input	PTM_09 - C1
14	Ground			Channel 13	Input	PTM_09 - C2
15	Ground			Channel 14	Input	PTM_09 - C3
16	Channel 15	Output	PTM_04 - O3	Channel 15	Input	PTM_10 - C1
17	Channel 16	Output	PTM_05 - O1	Channel 16	Input	PTM_10 - C2
18	Channel 9	Output	PTM_02 - O3	Channel 10	Output	PTM_03 - O1
19	Channel 11	Output	PTM_03 - O2	Channel 12	Output	PTM_03 - O3
20	Channel 13	Output	PTM_04 - O1	Channel 14	Output	PTM_04 - O2
21	Channel 1	Output	PTM_00 - O1	Channel 2	Output	PTM_00 - O2
22	Channel 3	Output	PTM_00 - O3	Channel 4	Output	PTM_01 - O1
23	Channel 5	Output	PTM_01 - O2	Channel 6	Output	PTM_01 - O3
24	Channel 7	Output	PTM_02 - O1	Channel 8	Output	PTM_O2 - O2
25	Channel 9 PIA	Input	PIA - PB0	Channel 10 PIA	Input	PIA - PB1
26	Channel 11 PIA	Input	PIA - PB2	Channel 12 PIA	Input	PIA - PB3
27	Channel 13 PIA	Input	PIA - PB4	Channel 14 PIA	Input	PIA - PB5
28	Channel 15 PIA	Input	PIA - PB6	Channel 16 PIA	Input	PIA - PB7
29	Channel 1 PIA	Input	PIA - PA0	Channel 2 PIA	Input	PIA - PA1
30	Channel 3 PIA	Input	PIA - PA2	Channel 4 PIA	Input	PIA - PA3
31	Channel 5 PIA	Input	PIA - PA4	Channel 6 PIA	Input	PIA - PA5
32	Channel 7 PIA	Input	PIA - PA6	Channel 8 PIA	Input	PIA - PA7

(*), Global zero volt detect (a16) connects to the following: PTM_00 - C1,C2,C3; PTM_01 - C1,C2,C3; PTM_02 - C1,C2,C3; PTM_03 - C1,C2,C3; PTM_04 - C1,C2,C3; PTM_05 - C1; PTM_10 - C3.

3.9.1 Switch settings and connections - TIO-33 boards.

The board base address is set by means of a 6-way D.I.L. switch. This should be set as follows:

Switch	
1	Off
1	Off
1	On
1	On
1	Off
1	Off

External connections to stepper drives are taken of the DIN 41642 connector at the rear of the board, as follows:

Ground	Pin 2a
Channel 3 pulse o/p	Pin 21a & 2c
Ground	Pin 3a
Channel 3 direction o/p	Pin 25c & 3c
Ground	Pin 4a
Channel 4 pulse o/p	Pin 21c & 4c
Ground	Pin 5a
Channel 4 direction o/p	Pin 26c & 5c
Ground	Pin 6a
Channel 5 pulse o/p	Pin 22c & 6c
Ground	Pin 7a
Channel 5 direction o/p	Pin 27c & 7c
Ground	Pin 8a
Channel 6 pulse o/p	Pin 23a & 8c
Ground	Pin 9a
Channel 6 direction o/p	Pin 28c & 9c

In addition Pins 1a and 1c need to be shorted together.

3.10 G-64 bus, 2 slot (PC3/152)

The 2 slot G-64 (PC3/152) is designed to be mounted in a standard 19" racking system. It has a Klippon type 4-way (optionally 6-way) connector for the power supply. The connections are as follows:

3.10.1 Connector 1 (4-way) power supply lines. 4 way Klippon connector.

1	-15/12 volts
2	+15/12 volts
3	+5 volts
4	0 volts

3.10.2 Connector 1 (6-way) power supply lines (Optional). 6 way Klippon connector.

1	+5 volts battery
2	-5 volts
3	-15/12 volts
4	-15/12 volts
5	+5 volts
6	0 volts

The -5v supply can be derived from the -15/12 volt supply, if Q1, C1 & C2 are installed.

3.11 G-64 bus & power supply, 3 slot (PC3/153)

The 3 slot G-64 (PC3/153) is designed to be mounted in a custom made enclosure. In addition to providing a G-64 bus, it also allows additional i/o for the PC3/100 rev F boards, and an integrated linear power supply.

The connections are as follows:

3.11.1 Connector 1 10-way 3·5mm Klippon connector for stepper control

1	0 volts DC input
2	24 volts DC input
3	Stepper host channel 2 direction
4	Stepper host channel 2 clock
5	Stepper host channel 1 direction
6	Stepper host channel 1 clock
7	Stepper host channel 4 direction
8	Stepper host channel 4 clock
9	Stepper host channel 3 direction
10	Stepper host channel 3 clock

3.11.2 Connector 2 10-way 3·5mm Klippon connector for stepper control

1	0 volts DC input
2	24 volts DC input
3	Stepper slave channel 2 direction
4	Stepper slave channel 2 clock
5	Stepper slave channel 1 direction
6	Stepper slave channel 1 clock
7	Stepper slave channel 4 direction
8	Stepper slave channel 4 clock
9	Stepper slave channel 3 direction
10	Stepper slave channel 3 clock

3.11.3 Connector 7 25-way D-connector(male) for keypad i/o.

1	Scan output to keypad no 1
2	Scan output to keypad no 2
3	Scan output to keypad no 3
4	Scan output to keypad no 4
5	Scan input from keypad no 1
6	Scan input from keypad no 2
7	Scan input from keypad no 3
8	Scan input from keypad no 4
9	0 volts DC
10	Scan input from keypad no 5
11	Scan input from keypad no 6
12	Scan input from keypad no 7
13	Scan input from keypad no 8
14	Scan input from keypad no 9
15	Scan input from keypad no 10
16	Scan input from keypad no 11
17	Scan input from keypad no 12
18	Scan input from keypad no 13
19	Scan input from keypad no 14
20	Scan input from keypad no 15
21	Buzzer output
22	0 volts DC
23	Input from IBM AT keyboard clock
24	Input from IBM AT keyboard data
25	+5 volts DC

3.11.4 Connector 22 9-way S.I.L. header for keypad i/o.

1	Scan output to keypad no 1
2	Scan output to keypad no 2
3	Scan output to keypad no 3
4	Scan output to keypad no 4
5	Scan input from keypad no 1
6	Scan input from keypad no 2
7	Scan input from keypad no 3
8	Scan input from keypad no 4
9	0 volts DC

3.11.5 Connector 24 4-way S.I.L. header for IBM AT keyboard.

1	0 volts DC
2	Input from IBM AT keyboard clock
3	Input from IBM AT keyboard data
4	+5 volts DC

3.11.6 Connector 9. 15-way D-connector(female) for LCD/VFD display.

1	+5v
2	0v
3	Address 0
4	Variable power supply for LCD
5	E clock
6	R/W
7	Data 1
8	Data 0
9	Data 3
10	Data 2
11	Data 5
12	Data 4
13	Data 7
14	Data 6
15	+5 volts DC or Chip select for display

3.11.7 Connector 25. 16-way D.I.L. header for LCD/VFD display.

1	+5v
2	0v
3	Address 0
4	Variable power supply for LCD
5	E clock
6	R/W
7	Data 1
8	Data 0
9	Data 3
10	Data 2
11	Data 5
12	Data 4
13	Data 7
14	Data 6
15	Reset
16	+5 volts DC or Chip select for display

3.11.8 Connector 26. 16-way S.I.L. header for LCD/VFD display.

1	0v
2	+5v
3	Variable power supply for LCD
4	Address 0
5	R/W
6	E clock
7	Data 0
8	Data 1
9	Data 2
10	Data 3
11	Data 4
12	Data 5
13	Data 6
14	Data 7
15	+5 volts DC or Chip select for display
16	Reset

3.11.9 Connector 10. 9-way D-connector for RS-485/422 & Operator Interface power supply

1	Unregulated DC power supply output (6.5-9 volts DC)
2	Tx(A) & Rx(A) (RS485) or Tx(A) (RS422)
3	Rx(B) & Tx(B) (RS485) or Rx(B) (RS422)
4	No connection
5	0v isolated
6	Unregulated DC power supply output (6.5-9 volts DC)
7	Tx(B) & Rx(B) (RS485) or Tx(B) (RS422)
8	Rx(A) & Tx(A) (RS485) or Rx(A) (RS422)
9	0v isolated

3.12 G-64 bus & power supply, 3 slot (PC3/154)

The 2 slot G-64 (PC3/154) is designed to be mounted in a custom made enclosure. In addition to providing a G-64 bus, it also allows additional i/o for the PC3/100 rev F boards, and an integrated switched mode power supply.

The connections are as follows:

3.12.1 Connector 1 2-way 5mm Klippon connector for operator interface power supply (Optional)

1 0 volts DC output
2 9•5 volts DC output

3.12.2 Connector 2. 16-way D.I.L. header for LCD/VFD display.(optional)

1 +5v
2 0v
3 Address 0
4 Variable power supply for LCD
5 E clock
6 R/W
7 Data 1
8 Data 0
9 Data 3
10 Data 2
11 Data 5
12 Data 4
13 Data 7
14 Data 6
15 Reset
16 +5 volts DC or Chip select for display

3.12.3 Connector 3 10-way 3·5mm Klippon connector for stepper control (optional)

1 0 volts DC
2 Stepper host channel 1 clock (TTL line driver)
3 Stepper host channel 1 direction (TTL line driver)
4 Stepper host channel 2 clock (TTL line driver)
5 Stepper host channel 2 direction (TTL line driver)
6 Stepper host channel 3 clock (TTL line driver)
7 Stepper host channel 3 direction (TTL line driver)
8 Stepper host channel 4 clock (TTL line driver)
9 Stepper host channel 4 direction (TTL line driver)
10 5 volts DC

3.12.4 Connector 4. 16-way S.I.L. header for LCD/VFD display. (optional)

1	0v
2	+5v
3	Variable power supply for LCD
4	Address 0
5	R/W
6	E clock
7	Data 0
8	Data 1
9	Data 2
10	Data 3
11	Data 4
12	Data 5
13	Data 6
14	Data 7
15	+5 volts DC or Chip select for display
16	Reset

3.12.5 Connector 5. 15-way D-connector(female) for LCD/VFD display.(optional)

1	+5v
2	0v
3	Address 0
4	Variable power supply for LCD
5	E clock
6	R/W
7	Data 1
8	Data 0
9	Data 3
10	Data 2
11	Data 5
12	Data 4
13	Data 7
14	Data 6
15	+5 volts DC or Chip select for display

3.12.6 Connector 9 10-way 3·5mm Klippon connector for stepper control

1	0 volts DC
2	Stepper slave channel 1 clock (TTL line driver)
3	Stepper slave channel 1 direction (TTL line driver)
4	Stepper slave channel 2 clock (TTL line driver)
5	Stepper slave channel 2 direction (TTL line driver)
6	Stepper slave channel 3 clock (TTL line driver)
7	Stepper slave channel 3 direction (TTL line driver)
8	Stepper slave channel 4 clock (TTL line driver)
9	Stepper slave channel 4 direction (TTL line driver)
10	5 volts DC

3.12.7 Connector 10. 9-way D-socket (RS-422) & Operator Interface power supply

1	Unregulated DC power supply output (6.5-9 volts DC)
2	Rx(B) & Tx(B) (RS485) or Rx(B) (RS422)
3	Tx(A) & Rx(A) (RS485) or Tx(A) (RS422)
4	No connection
5	0v isolated
6	Unregulated DC power supply output (6.5-9 volts DC)
7	Rx(A) & Tx(A) (RS485) or Rx(A) (RS422)
8	Tx(B) & Rx(B) (RS485) or Tx(B) (RS422)
9	0v isolated

3.12.8 Connector 9. 9-way D-socket (RS-232) auxiliary port 1

1	Not used
2	RS-232 serial port TX - Output
3	RS-232 serial port RX - Input
4	Not used
5	RS-232 serial port GND
6	Not used
7	Not used
8	Not used
9	Not used

3.12.9 Connector 15. 9-way D-plug (RS-232) auxiliary port 3

1	Not used
2	Not used
3	RS-232 serial port RX - Input
4	RS-232 serial port TX - Output
5	RS-232 serial port GND
6	Not used
7	Not used
8	Not used
9	Not used

3.12.10 Connector 19 2-way 5mm Klippon connector for encoder power supply output

1	0 volts DC output
2	5 volts DC output

3.12.11 Connector 20 2-way 5mm Klippon connector for 24v power supply input

1	0 volts DC input
2	24 volts DC input

3.12.12 Connector 21. 9-way D-plug (RS-232) auxiliary port 2

1	Not used
2	Not used
3	RS-232 serial port RX - Input
4	RS-232 serial port TX - Output
5	RS-232 serial port GND
6	Not used
7	Not used
8	Not used
9	Not used

NOTE: Auxiliary port 1 is a 9 pin male RS-232 socket on the left hand side of the motherboard.
Auxiliary port 2 is a 9 pin female RS-232 or RS422 socket on the left hand side of the motherboard at the bottom.
Auxiliary port 3 is a 9 pin female RS-232 or RS422 socket on the left hand side of the motherboard one up from the bottom.

3.13 Analogue inputs, 8 channels isolated (PC3/155)

3.13.1 Connectors 1-8. 4-way 3·5mm Klippon connector for analogue inputs

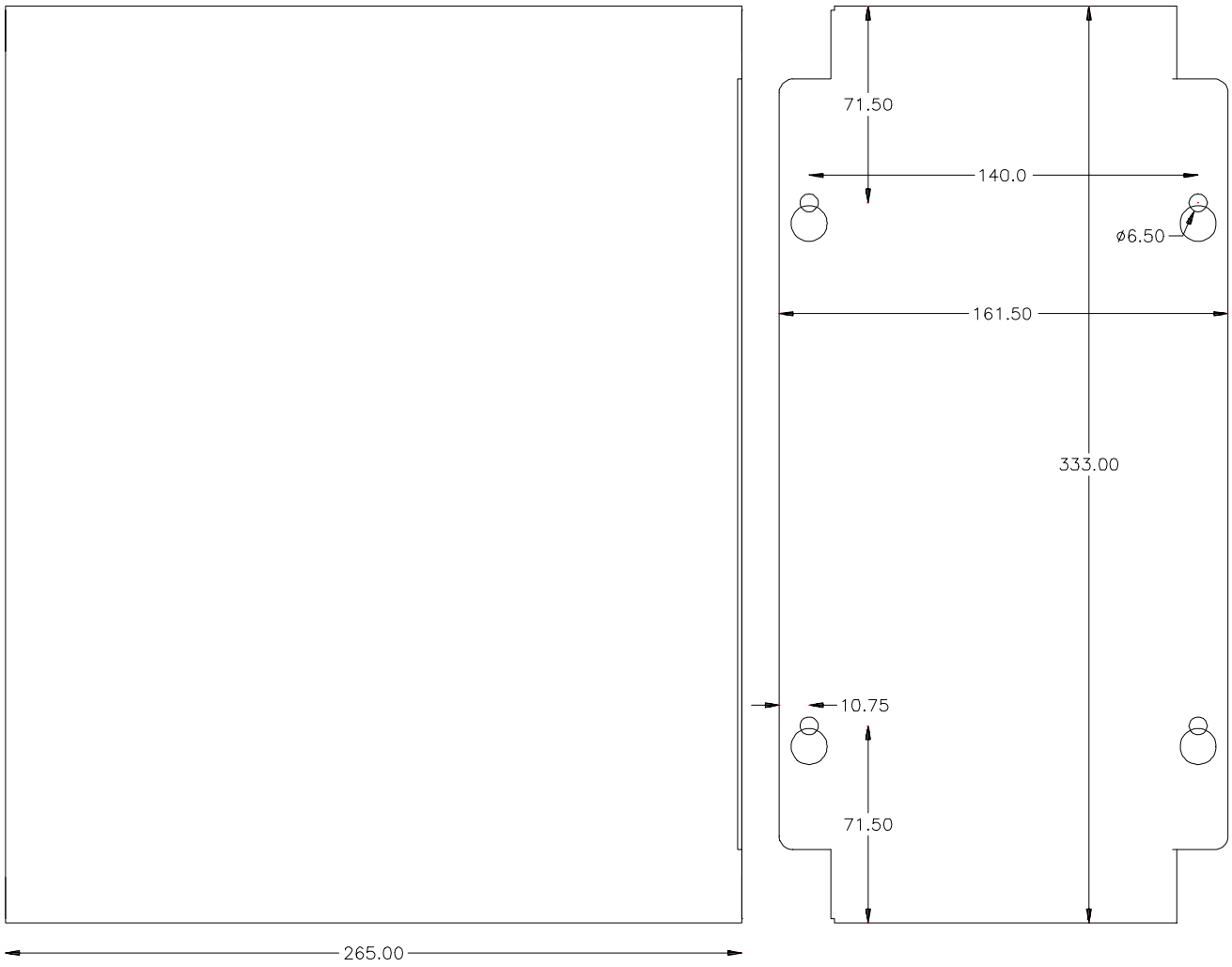
1	Ground supply for isolated input
2	Isolated input 0-10v or 0-±10v
3	+15v supply for isolated input
4	-15v supply for isolated input

3.13.2 Jumpers 1-8.

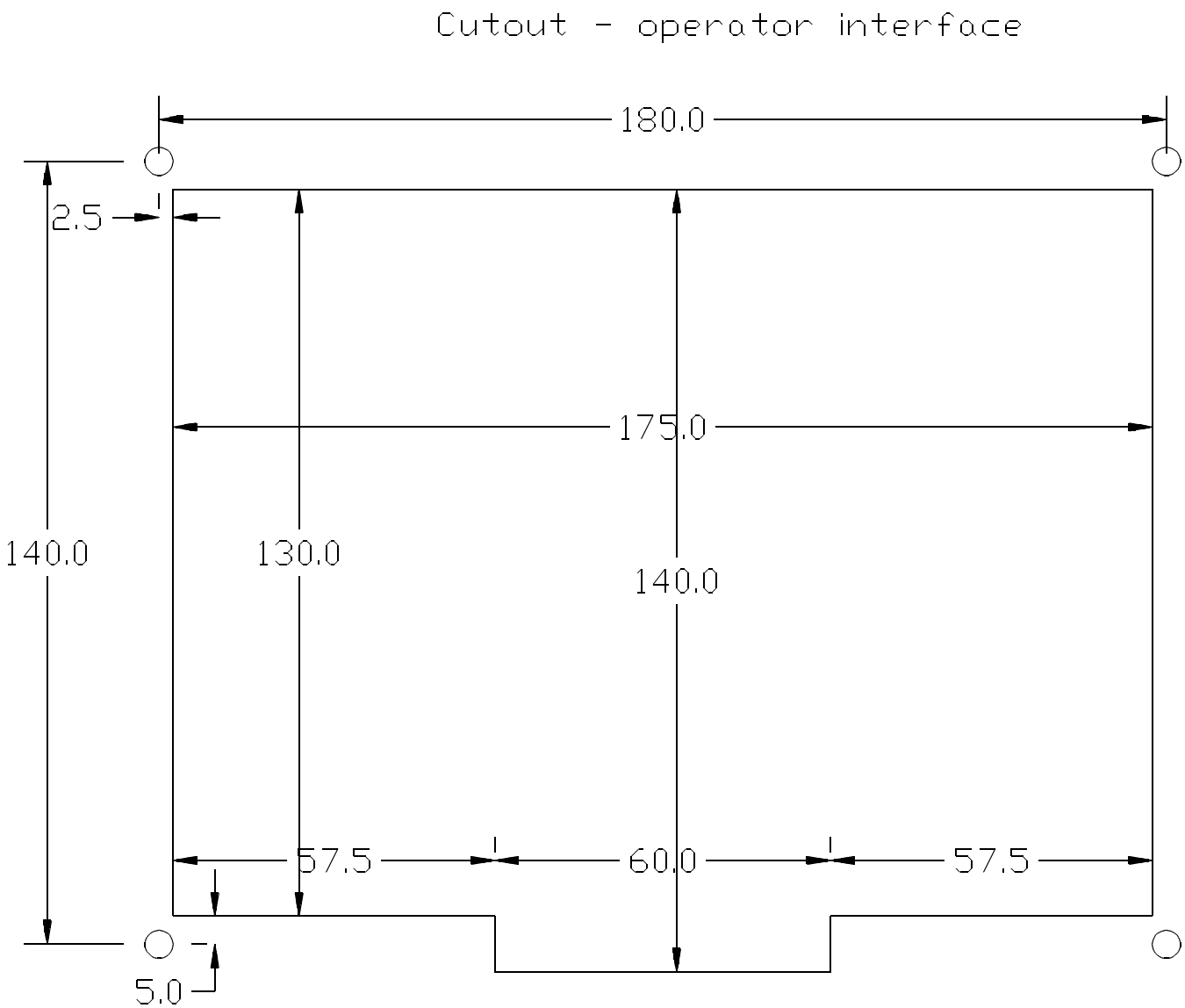
Jumper	Function	Connections
1-8	Bipolar 0-±10v analogue input	1-2
	unipolar 0-10v analogue input	2-3

4 DIMENSIONS

4.1 Main control system



4.2 Operator interface cutout



5 APPENDIX

5.1 Encoder connections to Contact 12-way connector

Pin	Wire	Function
1	Green	Pulse /B
2		
3	Orange	Pulse /Z
4	Blue	Pulse Z
5	Brown	Pulse A
6	Yellow	Pulse /A
7		
8	Red	Pulse B
9	Screen	Shield
10	Black	0v
11		
12	White	+5v

5.2 Encoder and analogue connections to PC3/100 and PC3/120 boards

Pin	Wire	Function
1	Brown	Pulse A
2	Yellow	Pulse /A
3	Red	Pulse B
4	Green	Pulse /B
5	Blue	Pulse Z
6		Spare
7		Spare
8	Black	0v Supply
9	White	+5v Supply
10	Orange	Pulse /Z
11	Blue (cable 2)	Velocity signal
12		Spare
13	Green (cable 2)	0v velocity
14	Red (cable 2)	Relay common
15	Yellow (cable 2)	Relay N.O.

6 INDEX

